

Description

Background of the invention:

[0001] This invention relates to a method of manufacturing a semiconductor device, and in particular, a method of forming an electrode of a compound semiconductor device, such as, a schottky junction field effect transistor (MESFET) and a hetero junction field effect transistor (HJFET).

[0002] Recently, devices which utilize high frequency of 0.5 GHz or more, such as, a portable telephone, a portable information terminal and a satellite communication / broadcast receiver have been widely used. In this event, a compound semiconductor device which is advantageous in performance, such as, electric power efficiency is used as the above device because a small size and lower power consumption are required in such devices.

[0003] Under such a circumstance, it is necessary that characteristics of the devices are uniform to each other to achieve designed performance in circuit devices which are mass-produced. The production of this device can not comply with manual adjustment of the characteristic in the course of a manufacturing step. Therefore, it is required to statistically control the step by the use of a processing apparatus having high accuracy, and namely to improve processing accuracy of each step. In addition, it is extremely important to apply a process which is capable of lowery suppressing variation of the characteristic.

[0004] In the general method of manufacturing the MESFET, a gate electrode is formed by the use of the dry etching, such as, the reactive ion etching (RIE). Specifically, a semiconductor layer is exposed by forming a gate opening in an insulating film by the use of the RIE. In this event, when the semiconductor layer is exposed on the condition that anisotropy is strong, the channel crystal layer is damaged due to ion impact. In consequence, carriers on the surface thereof are unevenly reduced. In this case, it is difficult to recover the damage by the heat treatment. Further, the manufacturing yield is degraded because the device characteristic of the FET becomes uneven.

[0005] To solve this problem, a variety of suggestions have been made about the anisotropy dry-etching method which utilizes microwave with low damage, such as, the electron cyclotron resonance (ECR). By the using the ECR method, the etching can be carried out under the low damage.

[0006] In the meanwhile, the epitaxial apparatus for the mass-production has been developed with advancement of the compound semiconductor device. In particular, it is possible to produce a thin-film having high impurity concentration by the use of the metal organic chemical vapor deposition (MOCVD) with high accuracy and reproducibility. In this condition, a fine gate electrode is arranged on the conductive semiconductor

layer of the thin-film having the high impurity concentration to produce the FET having high transconductance gm and cut-off frequency f_T with high reproducibility.

[0007] Therefore, the ECR dry etching has been attempted to be utilized by using the epitaxial semiconductor substrate which is fabricated by the use of the MOCVD. Namely, when the insulating film is etched or opened, the RIE method is first carried out until the insulating film of 100 nm is left so as to occur no damage for the semiconductor layer. Thereafter, the ECR method is performed to expose the semiconductor layer.

[0008] However, reacted product is generated on the surface of the semiconductor layer (namely, channel layer) after the etching. Where the reacted product is left on the shottky electrode forming region, a forward current does not flow even when the forward bias is applied by forming the shottky electrode. Therefore, an excellent shottky barrier is not formed in this condition. Consequently, the gate function can be obtained.

[0009] On the other hand, suggestion has been made about another method of forming the gate electrode. In this method, after the insulating film is left with the preselected region, the wet etching is carried out to expose the semiconductor layer. In this case, the two kinds of insulating films are deposited to prevent the opening from unevenly widening by the isotropic wet etching.

[0010] However, in this method, the side etching takes place in the insulating film by the use of the wet etching. Consequently, vaporized electrode metal is cut out with the step-shape in the side-etching portion.

[0011] Further, suggestion has been made about the other method of forming the gate electrode. In this method, a sloped side surface is used in order to improve the connection of the vaporized metal in the gate-opening portion. Thereby, a reduced gate opening which has the sloped side surface on an upper portion of the opening can be formed on the condition that the sloped curve surface is kept.

[0012] However, the side etching brings about in the bottom portion because the isotropic etching is carried out for the insulating film. Consequently, the vaporized metal does not almost enter into the opening. As a result, the metal of the side surface becomes thin and thereby, the series resistance becomes large.

[0013] As mentioned before, when the semiconductor layer (crystal surface of compound semiconductor) is exposed by the dry etching, the reacted product is formed by the crystal components and the carbon. Consequently, the excellent shottky barrier can not be formed.

[0014] Further, when the electrode is formed in the fine opening, it is difficult that the vaporized electrode metal entirely or completely attaches on the side surface. In consequence, the electrode inevitably becomes thin. As a result, the series resistance is increased and the disconnection of the electrode often take place.

Summary of the Invention:

[0015] It is therefor an object of this invention provide a method of manufacturing a compound semiconductor device which is capable of equalizing threshold voltages VT of FETs in a surface thereof or between wafers.

[0016] It is another object of this invention provide a method of manufacturing a compound semiconductor device which is capable of suppressing increase of series resistance of a fine electrode.

[0017] It is another object of this invention provide a method of manufacturing a compound semiconductor device which is capable of improving productivity of a compound semiconductor device.

[0018] According to this invention, a semiconductor device has a semiconductor substrate, a channel layer formed on the semiconductor substrate and an insulating film deposited on the channel layer. In this event, an opening corresponding to a gate electrode pattern is formed in the insulating film by the use of a photo-resist film. Herein, the channel layer contains crystal components while the photo-resist film contains carbon. In this condition, the insulating film is etched to expose the channel layer after removing said photo-resist film. In consequence, no reacted production is formed between the crystal components and the carbon on the exposed channel layer.

[0019] More specifically, the channel layer is formed on the semiconductor substrate. Further, the insulating film is deposited on the channel layer. Moreover, a photo-resist film is formed on the insulating film. In this event, the photo-resist film has a first opening corresponding to a gate electrode pattern.

[0020] Next, a second opening is formed in the insulating film by the use of a first etching process by using said photo-resist film as a mask. Consequently, the insulating film is left with a reselected thickness. Thereafter, the photo-resist film is removed.

[0021] Subsequently, the remaining insulating film is etched by the use of a second etching process so as to expose the channel layer. Finally, the gate electrode pattern is formed on the exposed channel layer.

[0022] In this case, the second etching process is lower in damage against the semiconductor substrate than the first etching process. For instance, the first etching process comprises the reactive ion etching (RIE) method. On the other hand, the second etching process comprises at least one selected from the group consisting of the electron cyclotron resonance (ECR) method; the inductive coupled plasma (ICP) method and the helicon method.

[0023] Thus, the opening is formed in the insulating film by the use of the photo-resist film on the condition that the insulating film is left with the preselected thickness. After the photo-resist film is removed, the remaining insulating film is removed by using the etching with the low damage. In consequence, the reacted product is not formed by the crystal components and the carbon

on the exposed channel layer. Therefore, the excellent shottky barrier can be formed between the exposed channel layer and the gate electrode pattern.

[0024] Further, it is unnecessary to add the oxygen to the etching gas or to additionally carry out the oxygen plasma process in order to avoid the generation of the reacted product. Thereby, the film reduction due to the oxidation of the crystal surface or the roughness of the surface can be prevented. Consequently, the threshold voltage V_T becomes shallow to keep the uniformity. This results in the improvement of the manufacturing yield.

[0025] Further, a slope is formed on the upper portion of the opening in this invention. Thereby, the vaporized electrode metal can be readily embedded in the opening via the slope, and the disconnection of the electrode can be avoided. In addition, the increase of the resistance can be effectively suppressed.

Brief Description of the Drawings:

[0026]

Figs. 1A through 1D are cross sectional views showing a method of a compound semiconductor device according to a first conventional example;

Fig. 2 is a cross sectional view for explaining a problem of a first conventional example;

Fig. 3 is a cross sectional 1 view for explaining a problem of a first conventional example;

Figs. 4A through 4D are cross sectional views showing a method of a compound semiconductor device according to a second conventional example;

Fig. 5 is a cross sectional 1 view for explaining a problem of a second conventional example;

Figs. 6A through 6D are cross sectional views showing a method of a compound semiconductor device according to a third conventional example;

Fig. 7 is a cross sectional view for explaining a problem of a third conventional example;

Fig. 8 is a cross sectional 1 view for explaining a problem of a third conventional example;

Fig. 9 is a cross sectional 1 view for explaining a problem of a third conventional example;

Fig. 10 is a cross sectional view showing a semiconductor compound device in an initial manufacturing step according to a first through seventh embodiments;

Fig. 11 is a layout diagram showing a compound semiconductor device, taken along A-A' line in Fig. 10;

Figs. 12A through 12D are cross sectional views showing a method of a compound semiconductor device according to a first embodiment;

Figs. 13A through 13D are cross sectional views showing a method of a compound semiconductor device according to a third embodiment;

Figs. 14A through 14D are cross sectional views

showing a method of a compound semiconductor device according to a fourth embodiment;

Figs. 15A through 15D are cross sectional views showing a method of a compound semiconductor device according to a seventh embodiment;

Figs. 16A through 16C are cross sectional views showing a method of a compound semiconductor device according to a eighth embodiment;

Figs. 17A through 17F are cross sectional views showing a method of a compound semiconductor device according to a ninth embodiment;

Figs. 18A through 18D are cross sectional views showing a method of a compound semiconductor device according to a tenth embodiment;

Figs. 19A through 19C are cross sectional views showing a method of a compound semiconductor device according to a tenth embodiment; and

Figs. 20A through 20C are cross sectional views showing a method of a compound semiconductor device according to an eleventh embodiment.

Description of the Preferred Embodiments:

[0027] Referring to Figs. 1 through 9, conventional methods of manufacturing compound semiconductor devices will be first described for a better understanding of this invention. The manufacturing methods are equivalent to the conventional manufacturing methods mentioned in the preamble of the instant specification.

(First conventional example)

[0028] A first conventional example is most general method of manufacturing the MESFET and is disclosed in Japanese Unexamined Patent Publication No. Hei. 6-45293.

[0029] Referring to Figs. 1A through 1D, description will be made about the first conventional example.

[0030] As illustrated in Fig. 1A, a channel layer (conductive semiconductor layer) 2 is formed on a semiconductor substrate 1 by the use of the known epitaxial growth method or the known ion implantation method. Herein, it is to be noted that the semiconductor substrate 1 is formed by the use of a semi-insulating GaAs substrate while the channel layer 2 is formed by an n-type GaAs.

[0031] Thereafter, an insulating film 4 which is formed by a silicon oxide film (SiO_2) is deposited on the channel layer 2 by the use of the known chemical vapor deposition (CVD) method. Subsequently, a photo-resist film 5 which has an opening corresponding to a gate electrode pattern is formed thereon, as shown in Fig. 1A.

[0032] Next, as illustrated in Fig. 1B, an anisotropy dry-etching process due to the reactive ion etching (RIE) method is carried out for the insulating film 4 by using the photo-resist film 5 as a mask. Thereby, a gate opening 6 is formed so as to expose a surface of the channel layer 2, as shown in Fig. 1B. Herein, mixed

gases with CHF_3 and O_2 is used in the RIE method.

[0033] Subsequently, the photo-resist film 5 operable as the mask is removed by the use of an organic solvent, as illustrated in Fig. 1C.

[0034] Successively, as shown in Fig. 1D, a metal film for forming a schottky junction with the exposed semiconductor layer is deposited by the use of the sputtering method or the vaporizing method due to the electron gun. Thereafter, the metal film is dry-processed by the use of the ion milling or the RIE method by using a photo-resist pattern (not shown) as a mask to form a gate electrode 7.

[0035] Next, although not shown in Fig. 1D, source and drain electrodes which ohmic-contact with the channel layer 2 are formed on both sides of the gate electrode 7. Thus, the MESFET is completed in the first conventional example.

[0036] Herein, description will be made about a principle of the RIE method. The principle is disclosed, for example, in "plasma chemistry in ULSI age", published by Kogyo Chosakai, pp. 86-87.

[0037] Specifically, a vicinity of an anode is in a plasma generating state containing ions and electrons in the glow discharge between the parallel fiat plates under low gas pressure. On the other hand, a vicinity of a cathode is negatively charged because emitted second electrons are collected. This phenomenon is called an ion sheath. Thereby, a large electric field is concentrated by a space electric charge.

[0038] In this condition, the etching process is carried out by the use of both the physicals sputtering effect and the chemical reaction. In this event, a cation is accelerated so as to impact with a substrate film in the physical sputtering effect while a radical absorbs on the substrate surface in the chemical reaction.

[0039] In this case, the etching becomes anisotropy because the acceleration is performed by the electric field due to the ion sheath. Therefore, damage takes place for the substrate by the impact with the accelerated ions. In this event, energy in addition to mass is also large because of the energy in the ion-state.

[0040] In the meanwhile, a voltage of the ion-sheath can be monitored, and is also called a self-bias voltage or a substrate voltage. In order to enhance the anisotropy by raising up the ion sheath voltage, the gas pressure must be lowered or a distance between the electrodes must be made narrow. In the reverse case, the self-bias voltage becomes small, and as a result, the damage against the crystal substrate can be weakened.

[0041] However, the anisotropy becomes weak to enhance the isotropic in the above-mentioned technique. In addition, the controllable ion-sheath voltage has a limit because the gas pressure which generates a stable glow discharge has a suitable range.

[0042] When the opening is formed in the insulating film by the use of the RIE method, if the semiconductor crystal surface is exposed on the condition that the anisotropy is strong by enhancing the ion sheath voltage,

the channel crystal layer is damaged by the ion impact. Consequently, the carriers near the surface are unevenly reduced. This damage can not be completely recovered by the heat treatment. As a result, the manufacturing yield is degraded because the device characteristic of the FET becomes uneven.

[0043] In order to avoid this problem, verification experiment was carried out on the condition that the etching process was first carried out under high anisotropy condition so that the insulating became thin. Thereafter, the etching process was finally performed on the condition that the ion sheath voltage was lowered by enhancing the gas pressure to form a final opening in the insulating film.

[0044] In this case, the conductive semiconductor layer which was formed by ion implantation or the epitaxial growth could not be accurately controlled. Therefore, the semiconductor layer was adjusted by making the semiconductor layer thick and grinding the semiconductor layer by the etching from the opening. Herein, the adjustment was carried out by measuring a current.

[0045] In this event, the surface of the semiconductor layer which was damaged could be etched. However, in this method, the productivity and the accuracy of the device characteristic were inevitably degraded. Further, it was difficult to improve performance, such as, transconductance g_m and cut-off frequency f_T by shortening the gate length and thinning the layer.

[0046] In the meanwhile, a variety of suggestions have been recently made about the anisotropy dry-etching methods which utilizes microwave with low damage by using a principle different from the parallel flat plate type RIE. For instance, these methods are disclosed in Proceeding titled "semiconductor world", March 1996, pp. 19-24 and the above-mentioned Proceeding, pp. 79-80.

[0047] These methods are classified into the electron cyclotron resonance (ECR) method, the inductive coupled plasma (ICP) method, and the helicon method in accordance with the principle for generating the plasma.

[0048] Thereinafter, the ECR method will be described in detail.

[0049] In the ECR method, the electron cyclotron resonance causes to be occur by applying the microwave to electrons in a magnetic field. Thereby, plasma having high density can be obtained under the low gas pressure in comparison with the RIE.

[0050] In the ECR etching, moving directions of the ions can be completed by placing the substrate in the ECR position. Thereby, the anisotropy can be strengthened by enlarging the mean free path under the low gas pressure. Further, the etching of the low damage is possible on the condition that the ion sheath is extremely low.

[0051] On the other hand, the epitaxial growth apparatus has been developed for the mass-production with the advancement of the compound semiconductor device. In particular, it is possible to produce a thin-film layer of high impurity concentration by the use of the

MOCVD method with the high accuracy and the excellent repeatability. In this condition, it is required to produce the FET having the transconductance g_m and the cut-off frequency f_T with the excellent repeatability by arranging the fine electrode on the conductive semiconductor layer of the highly-doped impurity concentration.

[0052] To this end, the ECR dry-etching method has been attempted by the use of the epitaxial semiconductor substrate which is fabricated by the MOCVD method. Specifically, the etching is carried out to cause to be occur no damage by the RIE method during opening the SiO_2 film so that the SiO_2 film of 100 nm is left. Thereafter, the etching is performed by the ECR method. In this event, the ECR dry-etching was carried out with gas which is mixed CF_4 with O_2 of 3% under the pressure of 1m Torr so that a polymer having strong polymerization degree does not take place on the SiO_2 film.

[0053] However, when the internal of the opening is observed after the above etching, a reacted production 16 brings about on the channel layer 2 (GaAs crystal surface), as illustrated in Fig. 2. As a result of Auger analysis, it is confirmed that the reacted production 16 is formed by Ga, As as the crystal components, and carbon.

[0054] Such a reacted production does not melt by the organic washing process or the dilution hydrochloric acid and is left on the channel layer 2, as shown in Fig. 2. When the reacted production is left in the schottky electrode forming region of the gate, even if the forward bias is applied to the schottky electrode, the forward current does not flow. In consequence, an excellent schottky barrier can not be formed in this state. As a result, the gate function can not be obtained.

[0055] To this end, when ashing process due to oxygen plasma is carried out for the reacted product 16, the semiconductor crystal is oxidized in addition to the reacted product 16. In this condition, when the reacted product 16 is removed by dissolving in the dilution hydrochloric acid, grooves 17 take place on the crystal surface of the channel layer 2, as illustrated in Fig. 3. Consequently, the surface of the channel layer 2 becomes rough.

[0056] Further, when the channel layer 2 becomes thin by oxidizing and melting, the threshold voltage V_T of the FET becomes shallow to degrade the uniformity. Such a reacted production 16 brings about even when SF_6 gas containing no carbon is used.

[0057] When oxygen rate which is mixed in the ECR dry etching is 10 % or more as the other method, generation of the reacted production is suppressed. However, the semiconductor crystal is oxidized, and the oxide is etched by melting in the dilution hydrochloric acid, like the above-mentioned plasma process. Moreover, the above-mentioned phenomenon occurs when the semiconductor surface is exposed on the condition that the gas pressure is increased and the ion sheath voltage is lowered by the RIE method.

[0058] In addition, it has been confirmed that the phenomenon that the reacted product 16 is formed by the above crystal components and the carbon is generated in an InP based crystal other than the GaAs based crystal.

(Second conventional example)

[0059] Another suggestion has been made about the method of forming the gate electrode in the above-mentioned Japanese Unexamined Patent Publication No. Hei. 6-45293. Specifically, two kinds of insulating films which are different from each other in the etching performance are deposited to solve a problem that an opening is unevenly widened by the isotropic wet-etching.

[0060] Referring to Figs 4A through 4D, description will be made about the second conventional example.

[0061] As illustrated in Fig. 4A, a channel layer 2 is formed on a semiconductor substrate 1. Next, a first insulating film 14 and a second insulating film 15 are successively deposited on the channel layer 2, as shown in Fig. 4A. Herein, it is to be noted that the first insulating film 14 is formed by a silicon oxide film (SiO_2) while the second insulating film 15 is formed by a silicon nitride film (SiN_x). Thereafter, a photo-resist film 5 which has an opening for a gate forming region is formed thereon, as shown in Fig. 1A.

[0062] Subsequently, a gate opening 6 is formed in the second insulating film 15 by the use of the RIE method, as illustrated in Fig. 4B. Herein, the RIE method is carried out by using a mixed gas with CHF_3 and O_2 . In this event, the first insulating film 14 is left because etching rate is slow, as illustrated in Fig. 4B.

[0063] Next, the first insulating film 14 is wet-etched by the use of buffered hydrofluoric acid which is mixed with ammonium fluoride to expose a surface of the channel layer 2. In this case, dimension of the gate opening 6 can be kept constant because the etching rate of the second insulating film 15 is slow.

[0064] Subsequently, the photo-resist film 5 is removed to form a gate electrode 7, as shown in Fig. 4D. In this example, the channel layer 2 is not damaged to suppress variation of the gate opening by making the first insulating film 14 thin (to 50 nm).

[0065] However, the side etching is carried out for first insulating film 14 (SiO_2) due to the wet etching in this example, as illustrated in Fig. 5. In consequence, the vaporized electrode metal 18 is cut out in the side-etching portion, as shown in Fig. 5.

(Third conventional example)

[0066] The other suggestion has been made about a method of forming a fine gate opening by using a sloped side surface to improve connection of a vaporized metal in the gate opening portion in Japanese Unexamined Patent Publication No. Sho. 63 - 174374.

[0067] Referring to Figs. 6A through 6D, description

will be made about the third conventional example.

[0068] As illustrated in Fig. 6A, a channel layer 2 is formed on a semiconductor substrate 1. Thereafter, an insulating film 4 is deposited on the channel layer 2. Further, a photo-resist film 5 which has an opening is formed on the insulating film 4.

[0069] Subsequently, the anisotropy dry etching is carried out for the insulating film 4 by using the photo-resist as a mask. Consequently, a gate opening 6 is formed in the insulating film 4, as shown in Fig. 1A.

[0070] Next, another insulating film 13 for forming a sidewall is deposited on the entire surface of the insulating film 4, as illustrated in Fig. 6B.

[0071] Subsequently, the anisotropy dry etching is carried out, as shown in 6C. Thereby, sidewall-insulating films 19 are formed in the gate opening 6 so as to form narrow gate opening 6a. Next, a gate electrode 7 is formed in the narrow gate opening 6a, as shown in Fig. 6D.

[0072] Thus, when another insulating film is deposited in a vertical opening in the insulating film, an edge of the opening portion becomes a curve surface. In this condition, when another insulating film is etched back by the use of the anisotropy dry etching, the sloped curve surface is left so that the narrow opening having the sloped side surface is formed in the opening portion.

[0073] However, it is assumed that an initial opening is narrow ($0.4\mu\text{m}$) and deep ($0.4\mu\text{m}$), as illustrated in Fig. 7. When an insulating film 13 for forming the sidewall is additionally grown, the insulating film 13 does not sufficiently reach a bottom portion because the upper portion becomes shadow. Consequently, the side surface becomes a reverse slope. When the insulating film 13 is etched back, a sidewall insulating film 19 is formed with the side surface of the reverse slope, as illustrated in Fig. 8.

[0074] In this event, the etching is carried out in the lateral direction in the bottom portion because the etching includes the isotropic other than the anisotropy. When an electrode metal 18 is vaporized under the opening shape, the vaporizing metal does not almost enter into the internal of the opening because the upper portion becomes shadow, as shown in Fig. 9. In consequence, the metal 18 of the side surface is thinned to increase the series resistance of the electrode.

[0075] As mentioned before, when the semiconductor layer (crystal surface of compound semiconductor) is exposed by the dry etching, the reacted product is formed by the crystal components and the carbon. Consequently, the excellent shottky barrier can not be formed.

[0076] To avoid this, when the oxygen plasma is applied, the crystal is also oxidized, and is ground by melting in the subsequent oxygen process. In consequence, the threshold voltage V_T becomes shallow so that the uniformity thereof is degraded.

[0077] Further, when the electrode is formed in the fine opening, it is difficult that the vaporized electrode

metal sufficiently attaches on the side surface. In consequence, the electrode inevitably becomes thin. As a result, the series resistance is increased and the disconnection of the electrode often takes place.

[0078] Taking the above-mentioned problems into consideration, this invention provides a method of manufacturing a compound semiconductor device which is capable of equalizing threshold voltages V_T of the FETs in the surface or between wafers and which is capable of suppressing an increase of series resistance of a fine electrode.

(Principle of this invention)

[0079] A principle of this invention will first be described for a better understanding of this invention.

[0080] When an opening is formed in an insulating film by the use of the dry-etching, such as, the ECR method using fluorine based gas by using a photo-resist film pattern as a mask, and thereby, a crystal surface of a compound semiconductor, such as, GaAs or InP, is exposed, the crystal surface is covered with a reacted product formed by compound semiconductor components and carbon, as mentioned before.

[0081] As a result of examination, it has been confirmed that the carbon is mainly supplied from the photo-resist film which is placed on the upper portion. More specifically, when the crystal surface is exposed, the semiconductor crystal which is activated by fluorine radical combines and reacts with the carbon other than the fluorine. This results in the reacted product on the exposed crystal surface. Further, the physical sputtering effect is weakened by lowering the ion sheath voltage in order to reduce the damage for the crystal surface. This is another factor that the reacted product is left.

[0082] Therefore, the crystal surface of the compound semiconductor is exposed after the photo-resist which supplies the carbon is removed in this invention. In this case, the crystal surface is exposed by etching back by the use of fluorine based gas containing no carbon, such as SF_5 or NF_3 , on the condition that the insulating film is left in the bottom portion of the opening.

[0083] Specifically, elements, such as, S, N, and other than the carbon does not strongly react with the compound semiconductor and, as a result, can be removed by melting the crystal to several nm by the use of the dilution acid process.

[0084] It is possible that hydrochloric is a source liquid of 36 % for the GaAs. However, soaking into the fine opening is improved by diluting with pure water. Further, it is desirable the source liquid of phosphoric acid is diluted to 10 % or less because the source liquid has extremely high viscosity at 85%. Sulfuric acid is undesirable because it melts the GaAs.

[0085] On the other hand, it is preferable to use liquid which is diluted phosphoric acid or sulfuric acid to 10% or less for the InP because the hydrochloric melts the crystal. Further, it is possible to perform the diluted

alkali process for total compound semiconductor. To this end, ammonium NH_4OH , ammonium fluoride NH_4F , ammonium sulfide $(\text{NH}_4)_2\text{S}$ can be used.

[0086] When gas which is added oxygen O_2 into gas containing the carbon, such as CF_4 , is used as the etching gas, generation of the reacted product of the carbon is suppressed. However, the compound semiconductor surface is oxidized and ground by melting in the subsequent acid process. In consequence, this process is inadequate.

[0087] Further, the chlorine-based gas containing chlorine, such as CCl_2F_2 or CCl_4 , is also undesirable to etch GaAs or InP of the compound semiconductor.

[0088] Moreover, the slope can be formed on the side surface of the insulating film opening in this invention. Specifically, the insulating film is etched to about half depth by the use of the RIE method having the strong anisotropy by using the photo-resist film as the mask. Thereafter, the insulating film is etched by withdrawing the photo-resist film in the lateral direction. Thereby, the insulating film of the withdraw portion of the photo-resist is etched to form the slope on the side surface of the opening.

[0089] It is possible to add oxygen into fluorine based gas, to enhance the pressure by the use of the fluorine based gas, to use the chlorine base gas, and to use gas which adds the fluorine based gas into the chlorine base gas, as the method for withdrawing the photo-resist film in the lateral direction.

[0090] Although the slope takes place on the upper portion of the insulating film by withdrawing the photo-resist, the original groove formed by the RIE method is kept in shape of thereof due to the anisotropy of the etching, and as a result, is transcribed to the lower portion of the opening even when the photo-resist is removed.

[0091] In this event, the etching gas pressure can be lowly kept in the first method for adding the oxygen. Consequently, the first method is most suitable because the anisotropy can be readily kept. On the other hand, the second method of enhancing the etching gas pressure is effective when the oxygen is not introduced.

[0092] As mentioned before, when the isotropic is increased in the etching, the side etching is carried out. The third chlorine based gas readily etches the photo-resist and easily becomes isotropic. To avoid this, it is effective that the fluorine base gas is mixed to weaken the effect of the chlorine.

[0093] It is possible to form the slope on the side surface at the upper portion of the opening in accordance with the method of withdrawing the photo-resist film in the course of the etching. Therefore, even when the opening becomes fine, the opening side surface can be covered with the electrode metal. As a result, the disconnection of the electrode metal or the increase of the resistance value can be prevented.

[0094] Subsequently, description will be made about embodiments of this invention with reference to the

drawings.

(First embodiment)

[0095] Referring to Figs. 10 through 12, a first embodiment will be described.

[0096] As illustrated in Fig. 10, a crystal layer is grown on a semiconductor substrate 1 which is formed by a semi-insulating i-type GaAs by the use of the MOCVD method or the MBE method. Specifically, a buffer layer 11 (an i-type GaAs) is deposited on the semiconductor substrate 1 to a thickness of 500nm. Next, a channel layer 2 (an n-type $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ having carrier concentration of $2.0 \times 10^{18} \text{cm}^{-3}$) is deposited on the buffer layer 11 to the thickness of 40 nm. Successively, a contact layer 3 (an n-type GaAs having carrier concentration of $4.0 \times 10^{18} \text{cm}^{-3}$) is deposited on the channel layer 2 to the thickness of 100 nm. Thereinafter, the buffer layer 11 will be abbreviated in the drawings except Fig. 10.

[0097] In this case, the channel layer 2 is controlled as follows. Namely, the substrate in which the contact layer 3 is not grown on the condition that the channel layer is deposited is taken out of the growth apparatus. Thereafter, aluminum (Al) is immediately vaporized thereon to form a schottky electrode by patterning to a preselected shape. Next, an ohmic electrode which is alloyed with an indium (In) is formed adjacent to the electrode.

[0098] Under this circumstance, the distribution characteristic of the carrier concentration is determined from the relationship (namely, C-V characteristic) between applied voltage and static capacitance to confirm the concentration of the doped carrier. In the control specification of the channel layer in the C-V characteristic, the doped carrier concentration and the accuracy are $2.0 \times 10^{18} \text{cm}^{-3}$ and $\pm 10\%$ under the applied voltage of 0V while the pinch-off voltage corresponding to the carrier concentration $1 \times 10^{16} \text{cm}^{-3}$ is $-1.3 \pm 0.20 \text{V}$.

[0099] In this event, after the FET is fabricated, the control is carried out so that the accuracy of the threshold voltage V_T is within the range of $\pm 0.15 \text{V}$. However, a simple measuring method of the static capacitance is used in the above control method. Consequently, the accuracy is lowered. In this case, 2σ is used as the \pm value of each accuracy. Herein, it is to be noted that the σ represents the standard deviation.

[0100] Further, with respect to the growth thickness, the buffer layer 11 is formed by repetition laminate layers of the i-type GaAs and the i-type AlGaAs, and the average repetition film thickness can be detected by the use of the measurement of X-ray. For example, each layer is grown with ten periods of 20 nm by the MOCVD of the rotation revolution type, and the film thickness accuracy of one period (40nm) can be set to $\pm 2 \text{nm}$.

[0101] Subsequently, a semiconductor device is fabricated by the use of the photolithography technique for the epitaxial growth semiconductor substrate.

[0102] As illustrated in Fig. 11, a photo-resist which covers a reverse pattern of a device separation region

21 is formed. In this condition, the device separation is carried out by the use of the ion implantation. Specifically, $^{11}\text{B}^+$ ions are doped under the acceleration-energy of 200 keV and doping dose of $1 \times 10^{13} \text{cm}^{-2}$. Thereby, defect causes to be occur in the device separation region to enhance the resistance.

[0103] Subsequently, a photo-resist film which covers a contact region 22 is formed, and a contact layer is processed, as shown in Fig. 10. Next, an insulating film is formed so as to cover the entire surface. Further, a photo-resist of an opening pattern of a gate opening 23 is placed to form the gate opening 23 by etching the insulating film.

[0104] Subsequently, an electrode metal is deposited to process to a pattern of a gate electrode 24. Thereafter, a photo-resist film which has an opening in a pattern of ohmic electrodes 25 and 26 is formed to open the insulating film. Further, the ohm metal is lifted off by the use of the photo-resist to form a source electrode 25 and a drain electrode 26. Thus, the formation step of the FET is completed. In this case, the gate opening 23 is placed near the source side.

[0105] Subsequently, description will be made about steps after the epitaxial growth substrate is completed with reference to Figs. 12A through 12D together with Figs. 10 and 11.

[0106] As illustrated in Fig. 10, a photo-resist 12 which corresponds to the contact region 22 in Fig. 11 is formed to etch the contact layer 3 by the dry etching. The etching is carried out by the ECR apparatus by using gas which mixes BCl_3 of 15 sccm with SF_6 of 5sccm (25%) under the pressure of 1mTorr. When the channel layer 2 is exposed, the etching is halted because aluminum fluoride AlF_x covers the surface. Herein, it is to be noted that etching selection rate between GaAs and AlGaAs is 100 times or more.

[0107] Subsequently, the photo-resist 12 is removed by the use of the organic solvent. In this event, fluoride layer is removed by immersing in the dilution hydrochloric for several minutes. Further, supersonic wave is applied in the organic washing. In this event, the washing is carried out in order of several times of methyl ethyl keton and isopropanol and, thereafter is dried. Herein, the dilution hydrochloric is a liquid of 20°C which mixes concentrated hydrochloric acid of 36% with pure water at a rate of 1:1.

[0108] Although the photo-resist 12 is used as the mask in the etching condition of the GaAs, the reacted product of the carbon causes no problem. This is because the etching rate between the GaAs and the photo-resist is high at 50 times and as a result, the etching quantity of the photo-resist is small. Further, the etching rate of the GaAs is rapid. Thereby, the etching power is small. Moreover, the photo-resist can be readily removed by the use of the organic solvent without hardening.

[0109] Subsequently, as shown in Fig. 12A, an insulating film 4 (namely, a silicon oxide film SiO_2) is depos-

ited to a thickness of 700 nm. Thereafter, a photo-resist film 5 which corresponds to the gate opening 23 illustrated in Fig. 11 is formed on the insulating film 4. In this event, the photo-resist film 5 has the thickness of about 1 μm and the opening lateral width of 1.0 μm .

[0110] Although not shown in Fig. 12A, a reflection prevention film is inserted below the photo-resist film 5 to improve exposure accuracy of the stepper. Herein, it is to be noted that a WSi film may be used as the reflection prevention film.

[0111] Next, the insulating film 4 is etched by the use of the parallel plate type RIE apparatus so that the film thickness of the insulating film 4 becomes about 100 nm. Thus, a gate opening 6 is formed in the insulating film 4 on the condition that a part of the insulating film 4 is left at the bottom portion, as illustrated in Fig. 12A. Herein, the etching is carried out by using a mixed gas of CF_4 with H_2 having flow rate of 20% under the gas pressure of 80nmTorr and the ion sheath voltage of 70V.

[0112] Subsequently, the photo-resist film 5 is removed by the use of the oxygen plasma, as shown in Fig. 12B. Successively, the organic washing is carried out. Thereafter, the remaining insulating film 4 is etched to 150 nm by the ECR dry etching so that the gate opening 6 penetrates to the channel layer 2. In this event, the etching is carried out by using SF_6 gas under the pressure of 1mTorr and the ion sheath voltage of 2V or less at the SiO_2 etching rate of 36 nm/min.

[0113] Thereafter, the organic washing and the dilution acid process are carried out, and a WSi_x is vaporized to the thickness of 200 nm by the sputtering process to form a schottky metal 10. In this case, the affect due to electrons and ions near the target can be suppressed by separating the semiconductor substrate from the sputter target with a preselected distance, for example, 15 cm or more. Next, the heat treatment is carried out at the temperature of 400°C for 30 minutes in the hydrogen atmosphere to recover a small damage. Successively, Ti having the film thickness of 30 nm and Au of the film thickness of 600 nm are vaporized by the sputtering to reduce the resistance.

[0114] Subsequently, a gate electrode 7 is formed by processing by the ion milling by the use of the pattern of the gate electrode 24 illustrated in Fig. 11, as shown Fig. 12D. Further, the insulating film 4 is opened by the buffered hydrofluoric acid by the use of the patterns of the ohmic electrodes 25 and 26 illustrated in Fig. 11. Next, AuGeNi which is the ohmic metal is vaporized and the lift off is carried out. Thereafter, a source electrode 8 and a drain electrode 9 are formed by alloying with the heat treatment, as illustrated in Fig. 12D.

[0115] In this case, about 80 of wafers which has a diameter of 76 mm (3 inch) were attempted. The threshold voltage of the obtained FET was $-0.92 \pm 0.15\text{V}$ (2σ) between batches due to the MOCVD growth and the internal of the wafer, and the maximum transconductance g_m was 360 mS/mm at the average. Further, the standard deviation σ of V_T inside the wafer surface was

within the range between 30 and 50 mV.

[0116] Moreover, the grinding of the channel layer 2 was about 3 nm in the etching of the contact layer 3, and 3nm in the opening formation of the insulating film 4 in accordance with the Transmission Electron Microscopy (TEM) observation after the device formation. Namely, the channel layer 2 is ground with 6 nm for the initial thickness 40 nm so that the thickness of 34 nm was left.

[0117] In this event, V_T of about 100 mV is changed for the change of the channel thickness of 1nm in V_T near this film thickness. Consequently, it is assumed that the total accuracy of the thickness is ± 1.5 nm from the above measurement result.

[0118] As the comparison experiment, as the thickness of the remaining insulating film (SiO_2) due to the initial RIE is thinned from 100 nm, when the film thickness becomes 50 nm or less, V_T is shallow by changing in the positive side. In consequence, the uniformity in the wafer surface is lowered. On the other hand, when the opening is formed on the condition that no SiO_2 film is left, the channel layer is damaged. Consequently, the carriers are eliminated so that the channel becomes non-conductive. Under this circumstances, the damage was not recovered by the use of the heat treatment of 400°C.

[0119] Therefore, although it is necessary that the thickness of the SiO_2 remaining film is 50 nm or more at which the damage starts to appear, the film thickness is set twice (to 100 nm), taking the etching accuracy of the RIE into consideration in this example.

[0120] As a second comparison experiment, the thickness of the SiO_2 remaining film in the RIE was set to 100 nm. In this condition, the remaining film was etched by the use of the ECR method on the condition that the photo-resist film was left. The etching quantity of the SiO_2 film was changed within the range between 150 and 300 nm. After the photo-resist film was removed by the use of the organic washing, the dilution acid process was carried out to form each electrode like the first embodiment.

[0121] In consequence, it was difficult that the current flowed (namely, almost non-conductive state). As a result, the voltage current characteristic was uneven in the forward direction in the wafer surface. Further, the gate did not normally function in the characteristic between the gate voltage and the drain current. Consequently, the drain current was not almost variable in many cases. This was because the reacted product was left on the interface of the gate electrode independently of the etching quantity of the SiO_2 film.

[0122] Moreover, as a third comparison experiment, after the etching due to the ECR, the ashing process due to the oxygen plasma was carried out to remove the photo-resist film in the organic washing. Thereafter, the dilution acid process was performed to form each electrode. In this case, although the gate conductive characteristic in the forward bias was improved by the use of the plasma process for 10 minutes, non-conductive

samples remained.

[0123] Under this circumstance, when the plasma process was carried out for 30 minutes, the gate became conductive, and the gate characteristic became uniform. However, the threshold voltage V_T was shallow at -0.6 ± 0.2 V, and the σ value in the wafer surface became large in the range between 40 mV and 80 mV. This is because the internal surface is unevenly oxidized by the oxygen plasma process, and as a result, the surface was ground by melting by the acid process.

[0124] As a fourth comparison experiment, affect of the over-etching of the SiO_2 film due to the ECR method was examined in this embodiment.

[0125] The etching rate in the opening having the lateral width of $1.0 \mu\text{m}$ was small at about 5% as compared to 36 nm / min in the flat plane. Further, the SiO_2 etching quantity in the flat plane is changed to 150, 200, 250, and 300 nm for the SiO_2 film which is left in the opening. When five wafers were manufactured as an experiment, respectively, the average V_T / σ value became - 936/42 mV, - 928/39 mV, - 851/47 mV, and - 683/62 mV. It was assumed that V_T became shallow and uneven due to both effects of the damage against the channel crystal layer and the subsequent crystal grinding by the acid process. Even when the ECR method with the low damage was used, if the over-etching was large, an adverse affect brought about. In consequence, it is desirable that the over etching is as small as possible.

(Second embodiment)

[0126] As a fifth comparison experiment, the final etching of the insulating film 4 was carried out by the use of the parallel plate type RIE instead of the ECR method. In this event, the etching was carried out by using SF_6 gas under high gas pressure of 150 mTorr. Further, high frequency power was put into the minimum level at which the plasma is generated, and the ion-sheath voltage was reduced to 20 V. Herein, the etching rate of the SiO_2 film was 4nm / min.

[0127] In this circumstance, the etching quantity of the SiO_2 was changed to 150, 200, and 250 nm. When five wafers were manufactured as an experiment, respectively, the average V_T / σ value became - 927/46 mV, - 784/65 mV, and - 259/143 mV. As compared to the ECR method, V_T largely became shallow and the uniformity was degraded for the over-etching quantity of the SiO_2 film. This is because the ECR method is lower in the damage than the RIE method. However, if the over etching becomes small by reducing the ion sheath voltage, it is possible to utilize the RIE method although the margin is small.

(Third embodiment)

[0128] In the third embodiment, the gate opening becomes narrow by the sidewall insulating film and at

the same time, the slope is placed on the upper portion of the opening, like the third conventional example.

[0129] Referring to Figs. 13A through 13D, description will be made about the third embodiment.

[0130] As illustrated in Fig. 13A, a silicon oxide film is deposited to a thickness of 700 nm as an insulating film 4. Thereafter, a photo-resist film 5 which has an opening of a lateral width of $1.0 \mu\text{m}$ is formed thereon. Next, the insulating film 4 is etched by the use of the parallel plate type RIE apparatus so that the thickness of the reaming film becomes about 100 nm. Consequently, a gate opening 6 is formed on the condition that the insulating film 4 is partially left on the bottom portion.

[0131] Subsequently, the photo-resist film 5 is removed, and an insulating film 13 for forming a side wall film (SiO_2) is deposited to the thickness of 300 nm, as illustrated in Fig. 13B.

[0132] Next, the insulating film 4 is entirely etched by the use of the RIE so that the thickness of about 100 nm is left. Thereby, sidewall insulating films 19 are formed on side surface of the insulating film 4, as shown in Fig. 13C.

[0133] Successively, the insulating film 4 is etched to 200 nm by the use of the ECR dry etching so that a gate opening 6a penetrates to the channel layer 2. In this event, the gate opening 6a becomes narrow by the side-wall insulating film 19. The lateral dimension of this gate opening corresponds to the gate length at the bottom portion. Herein, the gate length is $0.6 \mu\text{m}$.

[0134] If the side wall insulating film which has the thickness equal to the thickness of the flat plane is merely formed, the gate length becomes $0.4 \mu\text{m}$. However, this difference is caused by the fact that the thickness of the side surface is thinner than that of the flat plane, and the etching is also carried out in the lateral direction in the ECR method.

[0135] Subsequently, each electrode is formed like the first embodiment, as illustrated in Fig. 13D. Thus, the FET is completed.

[0136] In this embodiment, the gate opening is reduced by the use of the side wall insulating film, and at the same time, the curve face on the upper portion of the gate opening formed by the side wall insulating is formed to improve embedding of the gate metal. The threshold voltage V_T of the obtained FET was -0.98 ± 0.15 V (2σ) between batches due to the MOCVD growth and the internal of the wafer, and the maximum transconductance gm was 420 mS /mm at the average. Further, the standard deviation σ of V_T inside the wafer surface was within the range between 30 mV and 50 mV. As compared to the first embodiment, V_T becomes deep and at the same time, gm is improved due to the short channel effect that the gate length is shortened from $1.0 \mu\text{m}$ to $0.6 \mu\text{m}$.

(Fourth embodiment)

[0137] Subsequently, description will be made about a

method of improving connection of a fine electrode without the sidewall insulating film with reference to Figs. 14A through 14D.

[0138] As illustrated in Fig. 14A, after a silicon oxide film having a thickness of 700 nm is deposited as an insulating film 4, a photo-resist 5 which has a short opening having an opening width of 0.4 μm and the thickness of 1 μm is formed thereon. In this event, a reflection prevention film (not shown) is inserted below the photo-resist film 5 to improve exposure accuracy of the stepper. Next, the etching is carried out by the use of the RIE to form a gate opening 6 using the photo-resist film 5 as a mask so that the insulating film 4 is left at half depth (about 300 nm). Herein, the etching is performed using CF_4 and H_2 of flow rate 20 % under the gas pressure of 80 mTorr.

[0139] Subsequently, another etching is additionally carried out by the ECR dry etching to thin the insulating film 4 in the gate opening 6 to the thickness of about 50 nm. In this case, this etching is carried out using gas which is mixed CF_4 of 14 sccm with oxygen O_2 of 6 sccm (30%) under the gas pressure of 1 mTorr.

[0140] Under this circumstance, the opening of the photo-resist film 5 is enlarged in the lateral direction by the etching, and at the same time, a slope is formed on the upper portion of the gate opening 6. However, the opening shape formed by the initial RIE is transcribed on the bottom portion of the opening by the etch-back even when the photo-resist film is removed.

[0141] In this event, the ECR dry etching has weak anisotropy under the low damage condition, as mentioned before. Thereby, the lateral dimension of the bottom portion is enlarged to 0.5 μm . Further, the lateral dimension of the upper portion of the gate opening 6 having the slope is about 1.2 μm .

[0142] Thereafter, the photo-resist film 5 is removed by the use of the ashing process due to the oxygen plasma, as shown in Fig. 14C. After, the organic washing is performed, the insulating film 4 is etched to 100 nm by the ECR dry-etching using SF_6 gas. Consequently, the surface of the channel layer 2 is exposed in the gate opening 6.

[0143] Subsequently, each electrode is formed like the first embodiment, as illustrated in Fig. 14D. Thus, the manufacturing step of the FET is completed.

[0144] The slope takes place on the upper portion of the gate opening 6 by withdrawing the photo-resist film 4. Thereby, the embedding of the metal is improved. Moreover, the insulating film 4 can be thinned immediately before the crystal surface is exposed because the etching is conducted by the ECR method having the low damage in comparison with the RIE method. Rather than, the thickness of the remaining film can be determined so that the crystal surface is not exposed from the uniformity of the deposited film and the etching uniformity of the RIE method and ECR method.

[0145] In the above embodiment, the deposited film is thin at the periphery of the wafer, and the etching rate is

rapid. Therefore, the thickness of the remaining film is set to 50 nm at the center portion. Consequently, the etch-back quantity can be reduced after the photo-resist film is removed. Further, the etching rate is not almost lowered in the bottom portion because the upper portion of the opening is enlarged by the slope.

[0146] The threshold voltage V_T of the obtained FET was $-1.03 \pm 0.15\text{V}$ (2σ) between batches due to the MOCVD growth and the internal of the wafer, and the maximum transconductance g_m was 440 mS/mm at the average. Further, the standard deviation σ of V_T inside the wafer surface was within the range between 30 and 60 mV. As compared to the first through third embodiments, although V_T became deep due to the short channel effect, the uniformity and the reproducibility were equal to the other embodiments.

(Fifth embodiment)

[0147] Description will be made about the case that the withdraw etching in the lateral direction is carried out by the use of the RIE method instead of the ECR method. Herein, the etching gas pressure is enhanced in the above RIE method.

[0148] The etching was performed by using CF_4 gas under high gas pressure of 150 mTorr on the condition that the ion sheath voltage was lowered to 40 V. In this case, the etching rate of the SiO_2 film was 18 nm/min. In this condition, the etching was conducted so that the insulating film is left to 100 nm on the bottom portion of the gate opening. In this event, the dimension of the bottom portion in the lateral direction was enlarged to about 0.6 μm . Further, the opening dimension of the upper portion of the opening was about 1.2 μm , and the slope was formed on the upper portion of the opening.

(Sixth embodiment)

[0149] The other gases which is capable of etching the insulating film (SiO_2) may be utilized as the gas for withdrawing the photo-resist film in the lateral direction because the etching is not performed so as to expose the semiconductor crystal. For instance, SF_6 or NF_3 are usable in the fluorine base, and may be added oxygen. Further, chlorine based gas may be usable because the etching rate of the insulating film is similar to the etching rate of the photo-resist or less so that the isotropic etching is readily performed.

[0150] However, it was difficult to control the etching of the photo-resist when the rate of the chlorine is high. Therefore, it was possible to adjust the shape by mixing the fluorine-based gas. For example, BCl_3 and CF_4 were mixed at the rate of 1:2.

(Seventh embodiment)

[0151] Referring to Figs. 15A through 15 D, description will be made about a seventh embodiment. In the

seventh embodiment, the connection for the fine electrode is improved by withdrawing the photo-resist opening in the lateral direction and the sidewall insulating film.

[0152] As illustrated in Fig. 15A, a silicon oxide film is deposited to a thickness of 700 nm as an insulating film 4, as illustrated in Fig. 15A. Thereafter, a photo-resist film 5 which has an opening having a opening width of 0.4 μm and the film thickness of about 1 μm is formed thereon. In this event, a reflection prevention film is inserted below the photo-resist film 5 to improve exposure accuracy of the stepper. Thereafter, the insulating film 4 is etched by the RIE method so that the insulating film 4 is left to half (300 nm).

[0153] Subsequently, the ECR dry etching is carried out for the insulating film 4. Thereby, the insulating film 4 is thinned to about 50 nm on the bottom portion of the opening, and at the same time, the slope takes place on the upper opening portion of the insulating film 4. Herein, it is to be noted that the ECR etching is performed by using a mixed gas containing CF_4 and oxygen O_2 of 30 % as the etching gas. In this condition, the lateral dimension of the formed gate opening is widened to 0.5 μm .

[0154] Subsequently, the photo-resist 5 is removed by the use of the oxygen plasma process, as shown in Fig. 15B. After the organic washing process is carried out, a SiO_2 is deposited to the thickness of 300 nm as an insulating film 13 for forming a sidewall film. In such deposition, the dimension of the lateral direction of the bottom portion of the opening becomes 0.1 μm . In this event, the thickness of the insulating film on the bottom portion of the opening becomes thinner than that of the flat surface portion.

[0155] Next, the SiO_2 film is etched to 100 nm on the bottom portion of the opening by the RIE method in which CF_4 gas and H_2 gas are used, as illustrated in Fig. 15C. In this event, the insulating film is etched to 20 nm in the flat portion while the etching rate is lowered in the opening because the opening is fine.

[0156] Successively, the insulating film 4 is etched to 200 nm at the flat surface portion using SF_6 by the use of the ECR dry etching. Thereby, a channel layer 2 is exposed in the gate opening 6a, as illustrated in Fig. 15C. In this case, the dimension in the lateral direction as the gate length is 0.2 μm on the bottom portion of the opening.

[0157] Subsequently, each electrode is formed like the first embodiment, as illustrated in Fig. 15D. Thus, the manufacturing step of the FET is completed. The withdraw in the lateral direction of the photo-resist and the slope by the sidewall insulating film are formed on the upper portion of the gate opening 6a. In consequence, the embedding of the gate metal is improved.

[0158] The threshold voltage V_T of the obtained FET was $-1.20 \pm 0.20 \text{ V}$ (2σ) between batches due to the MOCVD growth and the internal of the wafer, and the maximum transconductance g_m was 480 mS/mm at

the average. Further, the standard deviation σ of V_T inside the wafer surface was within the range between 50 and 90 mV. As compared to the other embodiments, the gate length became short to 0.25 μm . Thereby, V_T becomes deep due to the short channel effect. Consequently, the uniformity and the reproducibility were slightly degraded in comparison with the other embodiments.

(Eighth embodiment)

[0159] So far, description has been made about one stage recess gate structure in which the gate is placed on the flat bottom surface of the recess which is embedded in the semiconductor layer. This structure is characterized in that the drain withstand pressure and the gate reverse break-down voltage of the FET can be enhanced. This invention is not limited to the one stage recess structure, and is effective for double stage embedding gate structure in which the semiconductor layer is further embedded from the insulating film before the gate electrode is formed. For instance, this manufacturing method is disclosed in Japanese Unexamined Patent Publication No. Hei. 2-105540.

[0160] The double stage recess embedding structure is characterized in that the affect due to the surface depletion layer which extends from the surface of the semiconductor layer can be removed by embedding the gate in the semiconductor layer.

[0161] In the single stage recess gate structure, the surface depletion layer which extends to the gate side serves to enhance the withstand pressure. The electric charge state of the surface level on the semiconductor surface with respect to the surface depletion layer is variable in accordance with the operation state of the FET. In consequence, the waveform becomes dull in the sharp pulse amplification while the analog amplification factor is fluctuated in the low frequency side. In this event, in the single stage recess structure, if the bandwidth of the high frequency is limited and the bias state of the circuit is invariable, no problem occurs.

[0162] In the double stage recess embedding gate structure, the gate depletion layer is deeper than the surface depletion layer by embedding the gate in the semiconductor layer. Thereby, the amplification factor as the controllability of the channel current is enhanced, and the response and the frequency dependency in the pulse amplification is improved. Consequently, the wide bandwidth can be achieved. Reversibly, the break-down voltage of the drain is lowered, and the cut-off frequency as the high frequency characteristic is reduced due to the increase of the gate capacitance. Therefore, it is important to adjust each FET function characteristic by the depth of the second recess and the structure factor in accordance of requirement performance of the FET. In this invention, it is possible to form the second recess at the high accuracy because the contamination and the crystal grinding is small before the second recess is

formed.

[0163] Referring to Figs. 16A through 16c, description will be made about the eighth embodiment of this invention. In this embodiment, the thickness of the channel layer 2 (n-type $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$) is set to 50 nm instead of 40 nm, and becomes thick at 10 nm corresponding to the depth of the second recess.

[0164] As illustrated in Fig. 16A, a SiO_2 film 4 is etched back on the condition that no photo-resist is formed. An n-type AlGaAs channel layer 2 which is exposed from a gate opening 6 or 6a is washed by the use of the organic washing process and the dilution hydrochloric process. In this event, the gate length of the SiO_2 film opening is set to $0.4\mu\text{m}$.

[0165] Subsequently, a second recess 27 is formed by digging the n-type AlGaAs channel layer 2 to the thickness of 100 nm by the wet etching process, as illustrated in Fig. 16B.

[0166] Herein, it is to be noted that the wet etching is classified into two methods. In a first method, A liquid for crystal oxidation and B liquid for oxide layer removal are repeated. In this event, the A liquid has the temperature of 20°C with the dilution which is specified by excess oxide hydrogen water (31 wt%) : water = 1:50. On the other hand, the B liquid has the temperature of 20°C with the dilution which is specified by chlorine (36 wt%) : water = 1:5. In this case, the liquid vessel has the room temperature to enhance the control.

[0167] The wafer which is placed on a Teflon case is moistened with water washing for one minute. Thereafter, the wafer is immersed in the A liquid for one minute to oxide the crystal surface with the excess oxide hydrogen water, and the crystal oxide layer is removed with the dilution hydrochloric acid by immersing it in the B liquid after shower water washing for two minutes. In this event, in a sequence of a step of the shower water washing, the crystal of 2.3 nm was ground, and the crystal of about 10 nm was ground by repeating this step at four times.

[0168] The etching rate was actually conducted by repeating this step at ten times and observing the cross sectional of the sample with the scanning electron microscope (SEM). In this event, the average value was obtained by dividing the measured digging depth by the repeating number.

[0169] In the second method, the wet etching was performed by rotating the wafer. The liquid was prepared by the rate specified by phosphoric acid (85 wt%): the excess oxide hydrogen water (31 wt%): water = 4:1:200 and has the temperature of 20°C .

[0170] The wafer was placed in parallel by fixing the rear surface of the wafer by the vacuum chuck. After the wafer was moistened by splashing the pure water to the wafer, the wafer was rotated at low speed of 20 rpm, and at the same time, the pure water was splashed to the central portion of the wafer. Next, the pure water was halted, and the same time, the etching liquid was splashed into the central portion of the wafer to etch for

23 seconds.

[0171] Subsequently, at the same time that the etching liquid was halted, the pure water was splashed and was washed with water for 60 seconds. Thereafter, the pure water was halted, the rotation number of the wafer was raised up to 200 rpm and was centrifugal dried for 30 seconds.

[0172] The etching quantity can be accurately controlled by using such a fresh etching liquid and momentarily changing the liquid. In this event, the etching rate was actually measured by changing the etching time, observing the cross sectional of the sample with the scanning electron microscope (SEM) and measuring the digging depth. Herein, it is to be noted that the etching rate is 26 nm/min.

[0173] As illustrated in Fig. 16C, WSi is vaporized by the sputtering to form the schottky metal 10 and the respective electrodes by the use of the dilution hydrochloric process like the above-mentioned embodiments. In this case, the gate electrode 7 is embedded in the second recess 27, as shown in Fig. 16C. The second recess is shallow and has a small side etching. Thereby, the metal is embedded in the second recess by the vaporizing due to the sputtering. When the second recess becomes deep, the side etching inevitably takes place. Consequently, the metal is cut out in the step shape like the second conventional example illustrated in Fig. 5. Therefore, it is desirable the depth of the second recess is 50 nm or less from experience.

[0174] In this condition, 30 of wafers each of which had the diameter of 76 mm was manufactured as an experiment for each of the second recess methods. In this event, the first method of repeating the two liquids was carried out at every five wafers with the preselected interval. In consequence, the threshold voltage V_T of the obtained FET was $-1.96 \pm 0.18\text{V}$ (2σ), and the σ value was within the range between 30 and 60 mV in the wafer plane.

[0175] On the other hand, the second method of rotating the wafer was performed at every ten wafers with the preselected interval. In consequence, the threshold voltage V_T of the obtained FET was $-0.98 \pm 0.21\text{V}$ (2σ), and the σ value was within the range between 40 mV and 80 mV in the wafer plane. Thus, the second method had a trend that V_T was shallow in the central portion of the wafer.

[0176] In the first method, the internal plane σ value was within the range between 30 mV and 50 mV in the embodiment having the second recess. Further, the rate determining of the wet oxide was utilized. Consequently, the uniformity in the plane of the MOCVD epitaxial substrate was kept, and the wafer internal plane was uniformly etched.

[0177] In the second method, the etching quantity trends to be large because the etching liquid is splashed into the central portion of the wafer. However, the reduction of the etching due to contamination on the crystal surface and the crystal grinding due to the oxide plasma

process was suppressed. Consequently, the threshold voltage V_T was not extremely increased in comparison with $\pm 0.15V$ (2σ) of V_T distribution in the first, third and fourth embodiments. As a result, it is confirmed that the wet etching is almost uniformly carried out, and the second recess is formed with an excellent reproducibility.

(Ninth embodiment)

[0178] In this embodiment, this invention is applied for forming the opening in the third conventional example disclosed in Japanese Unexamined Patent Publication No. Sho. 63-174374. In this example, the recess is formed by side-etching the crystal from the opening of the insulating film. Further, after the sidewall insulating film is formed inside the recess, the gate electrode which is separated in the self-alignment manner from the crystal side surface by the sidewall insulating film is formed. In this condition, this invention is applied to the step of forming the opening of the initial insulating film.

[0179] Referring to Figs. 17A through 17F, description will be made about the ninth embodiment. Herein, the used epitaxial substrate is the same as that in the first embodiment. However, the contact crystal layer is not processed by using the photolithography described in the first embodiment. On the other hand, the device separation is carried out by using B^+ ion-implantation.

[0180] As illustrated in Fig. 17A, a silicon oxide film is deposited to the thickness of 700 nm as an insulating film 4 on an epitaxial growth substrate in which the device separation is carried out. Further, a photo-resist film 5 which has an opening having an opening width of $0.4\mu m$ and has the film thickness of $1\mu m$ is formed thereon. In this event, a reflection prevention film (not shown) is inserted below the photo-resist film 5 to improve exposure accuracy of the stepper.

[0181] Thereafter, a gate opening 6 having a slope portion on the upper portion is formed in the insulating film 4, like the fourth embodiment. Specifically, the insulating film 4 is opened to a preselected depth by the RIE method using CF_4 and H_2 . Moreover, the insulating film 4 is thinned to the thickness of about 50 nm on the opening bottom surface by the use of the ECR dry etching in which a mixed gas containing CF_4 and oxygen O_2 of 30 % is used. At the same time, the slope is formed on the upper portion of the opening of the gate opening 6. In this event, the lateral dimension of the opening bottom is widened to $0.5\mu m$.

[0182] Subsequently, the photo-resist film 5 is removed by the use of the oxygen plasma process, as shown in Fig. 17B. After the organic washing process is performed, the insulating film 4 is etched to 100 nm by the ECR method dry-etching using SF_6 to expose a contact layer 3 from the gate opening. Thereafter, the crystal surface of the semiconductor is washed by the use of the organic washing and the dilution hydrochloric.

[0183] Next, the contact layer (n-type GaAs layer) 3 is

etched by the use of the ECR method dry-etching, as illustrated in Fig. 17C. In this case, the etching is conducted by using a mixed gas of BCl_3 and SF_6 of 25% under the pressure of 1 mTorr. When the channel layer 2 (AlGaAs) is exposed, the etching for covering the surface of aluminum fluoride AlF_x is halted. After the organic washing process is performed, the fluoride layer is removed by immersing it in the dilution hydrochloric for several minutes.

[0184] Subsequently, a SiO_2 film is deposited to the thickness of 300 nm as an insulating film 13 for forming a sidewall film, as illustrated in Fig. 17D. In this deposition, the lateral dimension of the opening bottom portion of the contact layer 3 becomes $0.1\mu m$. In this event, the thickness of the insulating film on the opening bottom portion becomes thinner than that of the flat plane portion.

[0185] Successively, the SiO_2 film is etched on the opening bottom portion by the use of the RIE method using CF_4 gas and H_2 gas so that the SiO_2 film is left to about 100 nm, as shown in Fig. 17E. Thereafter, polymer or carbon is washed by the use of the oxygen plasma process and the organic washing process. Successively, the insulating film 4 is etched to 200 nm on the flat plane portion by the ECR method dry-etching using SF_6 gas. Thereby, the surface of the channel layer 2 is exposed from the gate opening 6. In this event, the dimension in the lateral direction as the gate length on the opening bottom portion becomes $0.2\mu m$.

[0186] Subsequently, each electrode is formed like the first embodiment, as illustrated in Fig. 17F. Thus, the forming step of the FET is completed. In this condition, the gate electrode is separated in the self-alignment manner from the contact layer by the sidewall insulating film to be thinned. Further, the slope brings about on the upper portion of the gate opening 6a due to the withdrawal in the lateral direction and the sidewall. Thereby, the embedding of the gate electrode is largely improved.

[0187] Under this circumstances, no etching defect occurs in the etching step (in Fig. 17C) of the contact layer using the insulating film 4 in which the gate opening 6 is formed as a mask because the reacted product is not attached.

[0188] The threshold voltage V_T of the obtained FET was $-1.20 \pm 0.15V$ (2σ) between batches due to the MOCVD growth and the internal of the wafer, and the maximum transconductance g_m was 530 mS/mm at the average. Further, the standard deviation σ of V_T inside the wafer surface was within the range between 40 mV and 80 mV. As compared to the seventh embodiment, the uniformity and the reproducibility were slightly improved, and g_m was also improved. This is because the source resistance is reduced by the self-alignment by the use of the sidewall insulating film.

[0189] In this case, although the recess is formed by the use of the dry-etching by arranging the etching halting layer at the intermediate portion of the semiconductor layer, the recess may be formed by the wet-etching

without the halting layer.

(Tenth embodiment)

[0190] Like in the ninth embodiment, the opening is inevitably widened in the lateral direction in the etch-back of the insulating film under the dry-etching condition which has weak anisotropy and low damage. When the fine gate electrode of about $0.1\mu\text{m}$ is formed, the accuracy of the final gate length is lowered by widening the opening. Consequently, the control of the insulating film processing step in the course must be enhanced. On the other hand, the grinding of the device semiconductor layer which is exposed at the step for forming opening in the insulating film is permitted because the etching halting layer of the device semiconductor layer is utilized in the ninth embodiment. Therefore, it is unnecessary to solve the defect in which the schottky barrier as mentioned in the conventional example is not formed.

[0191] Referring to Figs. 18A through 18D and Figs. 19A through 19C, description will be made about the tenth embodiment. Herein, it is to be noted that the connection of the fine electrode will be solved in the tenth embodiment. Further, the epitaxial growth substrate and the device separation due to B^+ ion-implantation are same as the ninth embodiment.

[0192] As illustrated in Fig. 18A, a silicon oxide film is deposited to the film thickness of 400 nm as a insulating film 4 on an epitaxial growth substrate in which the device separation is carried out. Thereafter, a photo-resist film 5 which has an opening having an opening width of $0.50\mu\text{m}$ and has the thickness of about $1\mu\text{m}$ is formed thereon. In this case, although the thickness of the silicon oxide film 4 is 700 nm in the ninth embodiment, the thickness is thinned without the etch back process in this embodiment.

[0193] Thereafter, the insulating film 4 is etched by the use of the RIE method using a mixed gas of CF_4 and H_2 having flow rate of 20% so that the insulating film 4 is left to half (180 nm). Thereby, the gate opening 6 is formed in the insulating film 4. In this event, the opening bottom portion is thinned to $0.44\mu\text{m}$ because polymer is attached on the side surface of the gate opening 6.

[0194] Subsequently, the silicon oxide film is etched to 270 nm by the ECR method dry etching using a mixed gas of CF_4 and oxygen O_2 of 30% under the pressure of 1 mTorr. Thereby, an n-type GaAs contact layer 3 is exposed on the bottom portion of the gate opening in the insulating film 4, as shown in Fig. 18B.

[0195] In this case, the dimension of the opening on the bottom portion in the insulating film 4 is $0.52\mu\text{m}$ while it is $0.98\mu\text{m}$ on the tapered upper portion. Further, the thickness of the insulating film 4 is thinned without the etch back so that the total etching quantity becomes small. Consequently, the widening in the lateral direction on the opening bottom portion is suppressed, and it is approximately identical with the film thickness dimen-

sion of the initial photo-resist. On the other hand, no carbon is attached to the exposed GaAs crystal surface because the etching gas contains oxygen. However, the surface is oxidized to several nm.

[0196] Subsequently, the remaining photo-resist film 5 is removed by the use of the ashing process due to the oxygen plasma, as illustrated in Fig. 18C. Thereafter, the washing process is carried out by the organic washing process and the dilution hydrochloric process. By this oxygen plasma process, the crystal surface of the n-type GaAs contact layer 3 is ground to about 10 nm with the dilution hydrochloric process. However, the original thickness of the contact layer 3 is 100nm, and the contact layer 3 is almost left.

[0197] Next, the contact layer 3 (the n-type GaAs) is etched by the ECR method dry-etching using a mixed gas of BCl_3 and SF_6 of 25% under the pressure of 1 mTorr, as illustrated in Fig. 18D. When the channel layer (AlGaAs) is exposed, the aluminum fluoride is generated, and thereby the etching is halted. After the organic washing process is performed, the fluoride layer due to the dilution hydrochloric process is removed. This process corresponds to the step illustrated in Fig. 17C.

[0198] Subsequently, as illustrated in Fig. 19A, a SiO_2 is deposited to the thickness of 300 nm as an insulating film 13 for a sidewall film. In this event, the lateral direction dimension of the opening bottom portion which is newly formed in the opening in the contact layer 3 is equal to $0.24\mu\text{m}$ in this deposition while the thickness of the SiO_2 in the vertical direction is equal to 220 nm.

[0199] As shown in Fig. 19B, the SiO_2 film is etched by 150nm by the RIE method in which H_2 of the flow rate having 20% is mixed with CF_4 so that the SiO_2 film is left about 100 nm at the opening bottom portion. Next, the polymer and the carbon are removed and washed by the use of the oxygen plasma process and the organic washing process. Successively, the insulating film 4 is etched with 200 nm at the fiat portion by the ECR method dry-etching using SF_6 gas. Thereby, the channel layer 2 is exposed in the newly formed gate opening 6a. In this case, the lateral direction dimension as the gate length is equal to $0.22\mu\text{m}$ at the opening bottom portion.

[0200] Subsequently, as illustrated in Fig. 19C, each electrode is formed like the first embodiment. Thereby, the FET is completed. In this event, pre-processing for vaporizing the gate metal by sputtering includes the organic washing process and the dilution hydrochloric process.

[0201] The lateral direction dimension of the opening bottom portion is equal to $0.22\mu\text{m}$, and the dimension continues with $0.16\mu\text{m}$ in the vertical direction. Consequently, the opening is gradually widened towards the upper portion so that the dimension is equal to $0.9\mu\text{m}$ at the highest portion. The gate electrode formed by WSi of 200 nm and Au of 600 nm is vaporized in the tapered opening to be embedded in the opening by the sputtering. As a result, the connection to the fine gate electrode

is excellently carried out without the disconnection.

[0202] The accuracy of the gate length (2σ) including the manufacturing lots was $\pm 0.026\mu\text{m}$ and $\pm 0.014\mu\text{m}$ in the ninth and tenth examples. The initial thickness of the insulating film was thinned without the etch-back. Thereby, the widening of the lateral direction at the opening bottom portion was suppressed and the accuracy of the gate length was improved.

[0203] When the gate length is shortened, the gate capacitance is reduced and the cut-off frequency f_T is improved. On the other hand, the gate reverse break-down voltage and the drain break-down voltage are reduced, and the reliability of the device is also reduced. When the limit shortest gate length is selected from the reliability, the setting center must become large with the accuracy in the case of bad accuracy. Thereby, the high performance is degraded. Therefore, it is desirable that the accuracy of the gate length is high.

[0204] In the meanwhile, the average maximum cut-off frequency in the device having the gate length of $0.22\mu\text{m}$, V_T of -1.1 V was equal to 90 GHz , the gate break-down voltage was -7 V , and the drain break-down voltage of the three terminals was 6 V .

[0205] The withdraw etching of the insulating film opening in the lateral direction is possible by increasing isotropic by enhancing the gas etching pressure without adding the oxygen, as mentioned in the fifth example. However, it is necessary to reduce the damage by lowering the ion-sheath voltage and by weakening the high frequency wave power to expose the crystal plane in the parallel plate type RIE, as described in the second example. On the other hand, the chlorine-based gas described in the sixth example can not be utilized in the tenth example because it etches the compound crystal. The usable gas is only fluorine-based gas, such as, CF_4 , SF_6 , and NF_3 which do not etch the compound crystal.

(Eleventh embodiment)

[0206] Although the single stage recess structure has been explained in the tenth embodiment, the double stage recess structure can be formed by digging the channel semiconductor layer before forming the gate electrode, as mentioned in the eighth embodiment.

[0207] Referring to Figs. 20A through 20C, description will be made about the eleventh embodiment.

[0208] An insulating film 4 is etched by the use of the ECR method dry-etching using SF_6 gas to expose the AlGaAs surface of the channel layer 2 from newly formed gate opening 6a. The surface is washed by the use of the organic washing process and the dilution hydrochloric process, as illustrated in Fig. 20A.

[0209] As shown in Fig. 20B, the n-type AlGaAs channel layer 2 is dug with 10 nm by the use of the wet-etching described in the eighth embodiment to form a second recess 27.

[0210] Subsequently, the formation step of the FET is

completed by forming each electrode like the first embodiment, as illustrated in Fig. 20C.

[0211] The contamination and the grinding of the crystal are small before arranging the second recess like the eighth embodiment. Thereby, the depth of the second recess can be accurately formed in the embodiment. Further, the gate length can have the high accuracy like the tenth embodiment. Moreover, the gate opening is gradually widened towards the upper portion by the taper formation. Consequently, the connection to the fine gate electrode can be carried out without the disconnection.

[0212] Description has been made about a simple hetero-junction field effect transistor (HJFET) which has the conductive semiconductor layer and the two-dimensional electron gas in the hetero-junction interface with the buffer layer for the comparison with the comparative examples in the above-mentioned embodiments. Herein, the channel layer is uniformly doped in the above conductive semiconductor layer.

[0213] However, this invention is not limited to these embodiments, and is applicable for the other compound semiconductors, such as the other type FET, diodes and hole devices.

[0214] Further, although description has been made about the ECR method as the dry-etching method having the low damage, the ICP method and the helicon method may be used instead of the ECR method to obtain the same effect.

Claims

1. A method of manufacturing a semiconductor device having a semiconductor substrate, comprising the following sequential steps of:

forming a channel layer on said semiconductor substrate;
depositing an insulating film on said channel layer;
forming a photo-resist film on said insulating film, said photo-resist film having a first opening corresponding to a gate electrode pattern;
forming a second opening in said insulating film by the use of a first etching process by using said photo-resist film as a mask so that said insulating film is left with a preselected thickness;
removing said photo-resist film;
etching the remaining insulating film by the use of a second etching process so as to expose said channel layer; and
forming said gate electrode pattern on said exposed channel layer.

2. A method as claimed in claim 1, wherein:

said second etching process is lower in dam-

age against said semiconductor substrate than said first etching process.

3. A method as claimed in claim 1, wherein:

said first etching process comprises the reactive ion etching (RIE) method.

4. A method as claimed in claim 1, wherein:

said second etching process comprises at least one selected from the group consisting of the electron cyclotron resonance (ECR) method, the inductive coupled plasma (ICP) method and the helicon method.

5. A method as claimed in claim 1, wherein:

said second etching process comprises the reactive ion etching (RIE) method.

6. A method as claimed in claim 1, wherein:

said semiconductor substrate comprises either one of a GaAs substrate and an InP substrate.

7. A method as claimed in claim 1, wherein:

said photo-resist is removed by the use of oxygen plasma.

8. A method as claimed in claim 1, wherein:

said exposed channel layer constitutes a shottky barrier with said gate electrode pattern.

9. A method as claimed in claim 1, further comprising the following step of:

forming a source electrode and a drain electrode at both sides of said gate electrode pattern.

10. A method of manufacturing a semiconductor device having a semiconductor substrate, comprising the following sequential steps of:

forming a channel layer on said semiconductor substrate;
depositing a first insulating film on said channel layer;
forming a photo-resist film on said first insulating film, said photo-resist film having a first opening corresponding to a gate electrode pattern;
forming a second opening in said insulating film by the use of a first etching process by using said photo-resist film as a mask so that said

insulating film is left with a preselected thickness;

removing said photo-resist film;
depositing a second insulating film on said first insulating film;
etching said second insulating film to leave sidewall film;
etching said remaining first insulating film by the use of a second etching process so as to expose said channel layer; and
forming said gate electrode pattern on said exposed channel layer.

11. A method as claimed in claim 10, wherein:

said sidewall film is formed so as to reduce said second opening in size.

12. A method as claimed in claim 10, wherein:

said side wall film constitutes a curve surface, and
the curve surface is formed so that said second opening is filled with said gate electrode pattern to improve connection between said gate electrode pattern and said channel layer.

13. A method as claimed in claim 10, wherein:

said second etching process is lower in damage against said semiconductor substrate than said first etching process.

14. A method as claimed in claim 10, wherein:

said first etching process comprises the reactive ion etching (RIE) method.

15. A method as claimed in claim 10, wherein:

said second etching process comprises at least one selected from the group consisting of the electron cyclotron resonance (ECR) method, the inductive coupled plasma (ICP) method and the helicon method.

16. A method of manufacturing a semiconductor device having a semiconductor substrate, comprising the following sequential steps of:

forming a channel layer on said semiconductor substrate;
depositing an insulating film on said channel layer;
forming a photo-resist film on said insulating film, said photo-resist film having a first opening corresponding to a gate electrode pattern;
forming a second opening in said insulating film

by the use of a first etching process by using said photo-resist film as a mask so that said insulating film is left with a first thickness;

forming a third opening having a slope in said insulating film by the use of a second etching process so that said insulating film is left with a second thickness;

removing said photo-resist film;

etching said remaining insulating film by the use of a third etching process so as to expose said channel layer; and

forming said gate electrode pattern on said exposed channel layer.

17. A method as claimed in claim 16, wherein:

said slope is formed so that said third opening is filled with said gate electrode pattern to improve connection between said gate electrode pattern and said channel layer.

18. A method as claimed in claim 16, wherein:

said first etching process comprises the reactive ion etching (RIE) method while each of said second etching process and said third etching process comprises the electron cyclotron resonance (ECR) method.

19. A method as claimed in claim 16, wherein:

each of said first etching process and second etching process comprises the reactive ion etching (RIE) method while said third etching process comprises the electron cyclotron resonance (ECR) method.

20. A method of manufacturing a semiconductor device having a semiconductor substrate, comprising the following sequential steps of:

forming a channel layer on said semiconductor substrate;

depositing a first insulating film on said channel layer;

forming a photo-resist film on said first insulating film, said photo-resist film having a first opening corresponding to a gate electrode pattern;

forming a second opening in said insulating film by the use of a first etching process by using said photo-resist film as a mask so that said insulating film is left with a first thickness;

forming a third opening having a slope in said insulating film by the use of a second etching process so that said insulating film is left with a second thickness;

removing said photo-resist film;

depositing a second insulating film on said first insulating film;

etching said second insulating film to leave sidewall films;

etching said remaining insulating film by the use of a third etching process so as to expose said channel layer; and

forming said gate electrode pattern on said exposed channel layer.

21. A method as claimed in claim 20, wherein:

said side wall film constitutes a curve surface, and

the curve surface is formed so that said third opening is filled with said gate electrode pattern to improve connection between said gate electrode pattern and said channel layer.

22. A method as claimed in claim 20, wherein:

said slope is formed so that said third opening is filled with said gate electrode pattern to improve connection between said gate electrode pattern and said channel layer.

23. A method as claimed in claim 20, wherein:

said first etching process comprises the reactive ion etching (RIE) method while each of said second etching process and said third etching process comprises the electron cyclotron resonance (ECR) method.

24. A method of manufacturing a semiconductor device which has a semiconductor substrate, a channel layer formed on said semiconductor substrate and an insulating film deposited on said channel layer, wherein:

an opening corresponding to a gate electrode pattern is formed in said insulating film by the use of a photo-resist film,

said channel layer contains crystal components while said photo-resist film contains carbon, and

said insulating film is etched to expose said channel layer after removing said photo-resist film so that no reacted production is formed between the crystal components and the carbon on the exposed channel layer.

FIG. 1A
PRIOR ART

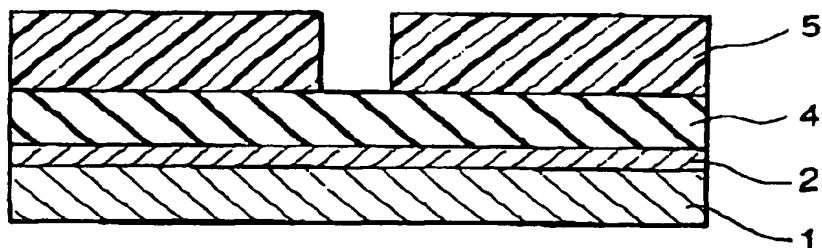


FIG. 1B
PRIOR ART

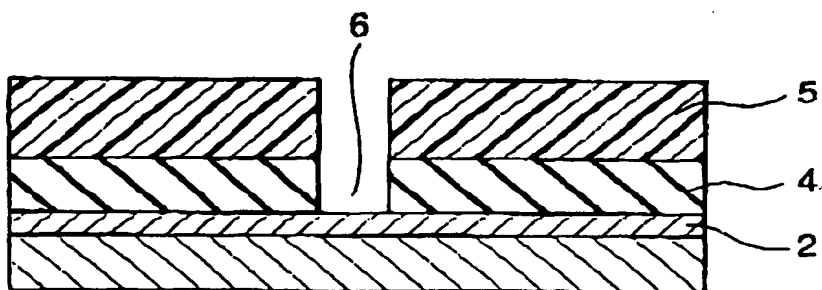


FIG. 1C
PRIOR ART

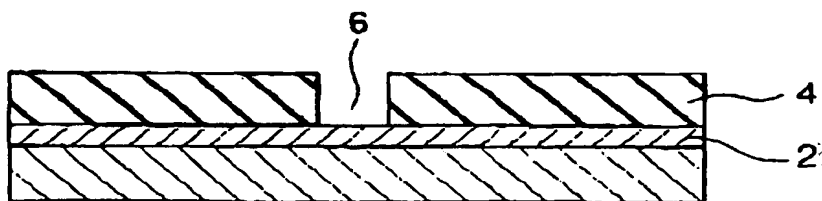
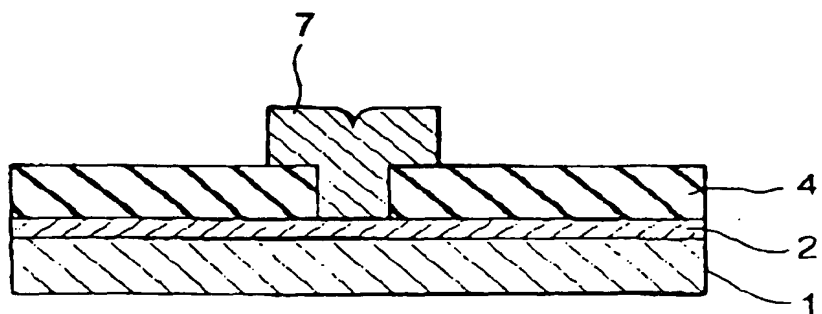


FIG. 1D
PRIOR ART



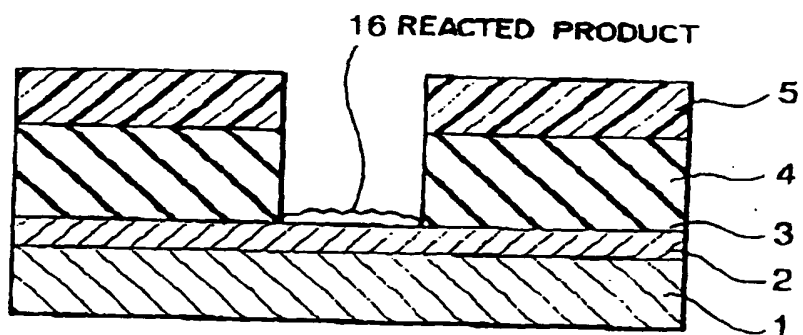


FIG. 2
PRIOR ART

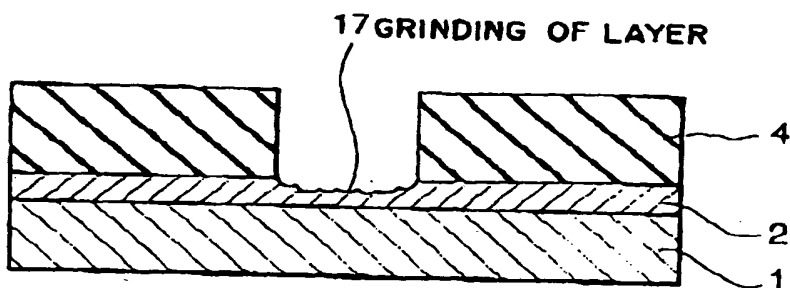


FIG. 3
PRIOR ART

FIG. 4A
PRIOR ART

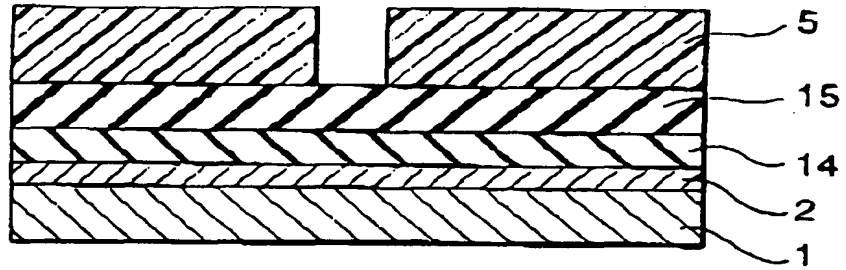


FIG. 4B
PRIOR ART

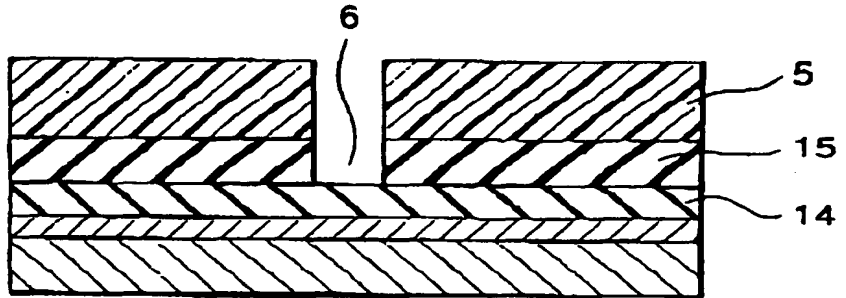


FIG. 4C
PRIOR ART

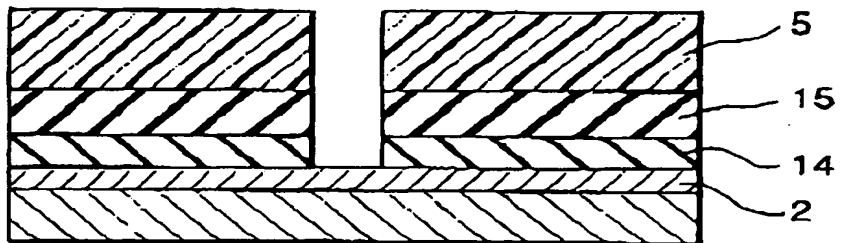
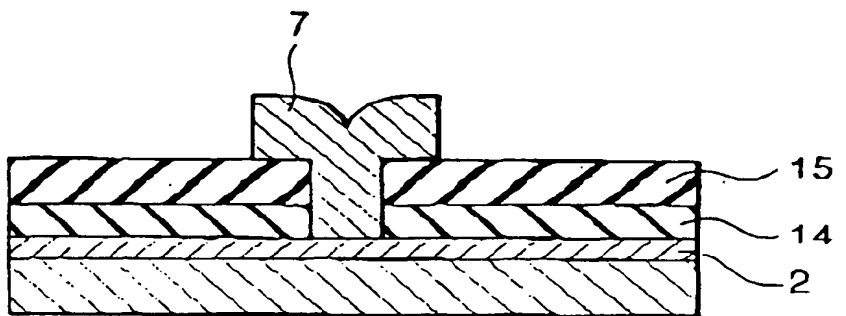


FIG. 4D
PRIOR ART



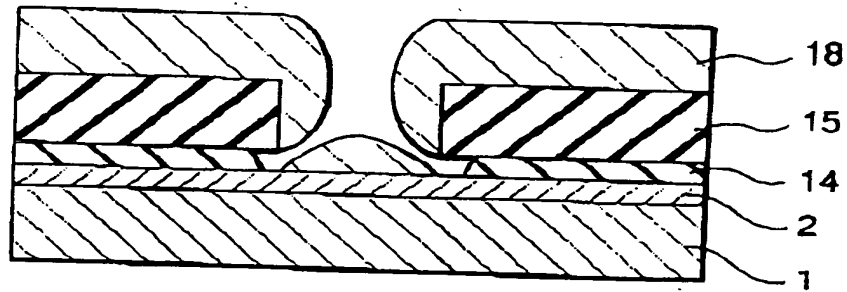


FIG. 5
PRIOR ART

FIG. 6A
PRIOR ART

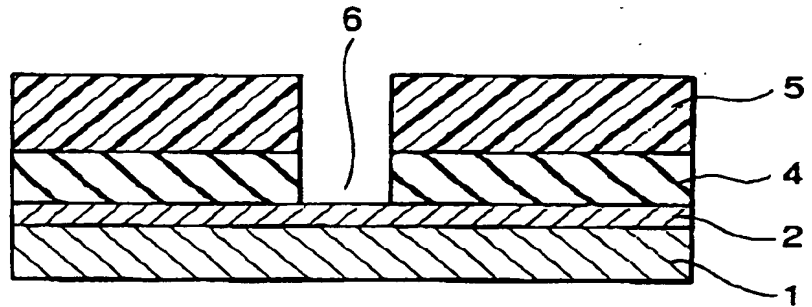


FIG. 6B
PRIOR ART

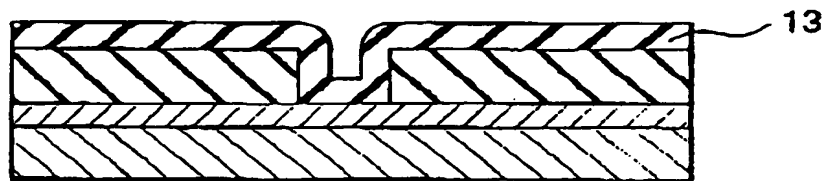


FIG. 6C
PRIOR ART

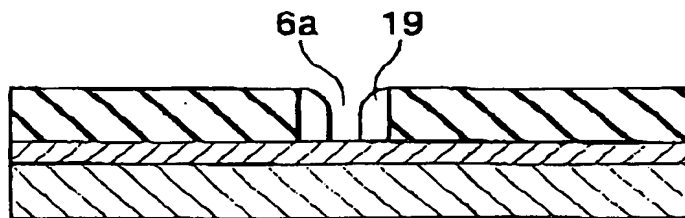
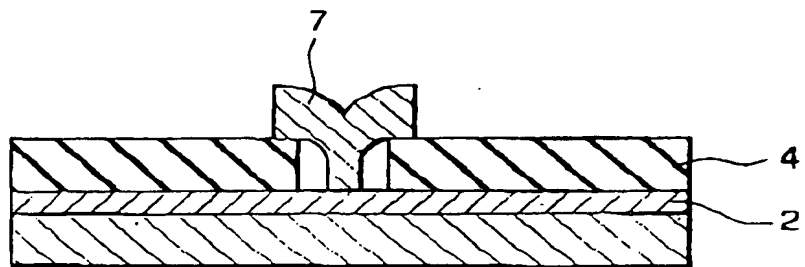


FIG. 6D
PRIOR ART



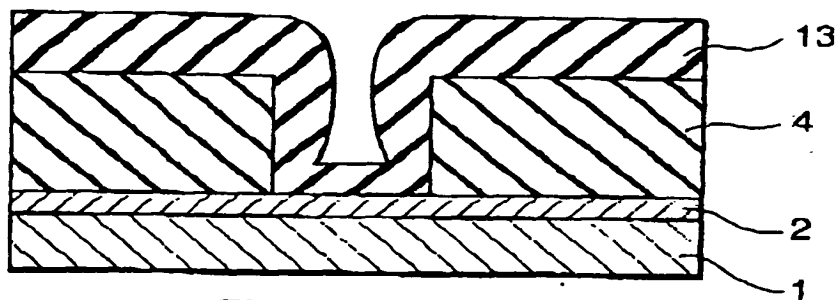


FIG. 7
PRIOR ART

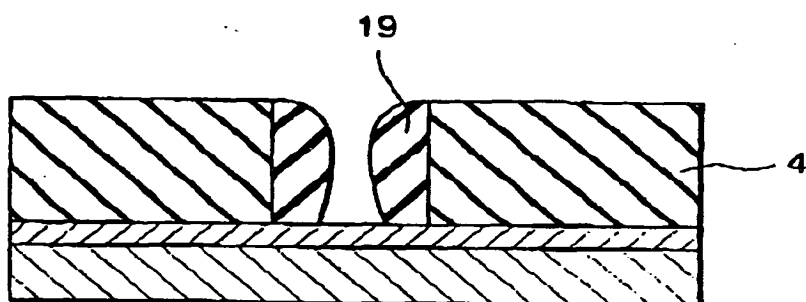


FIG. 8
PRIOR ART

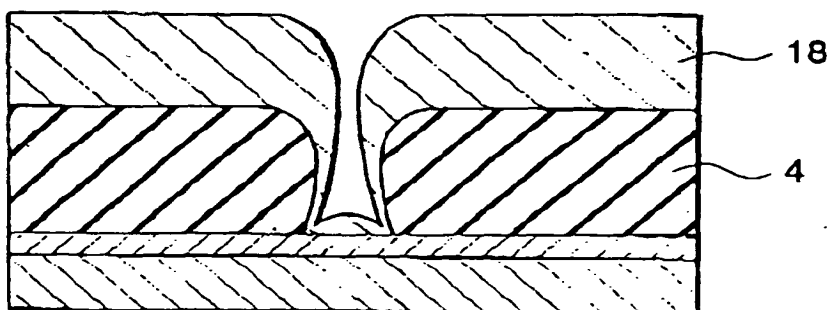


FIG. 9
PRIOR ART

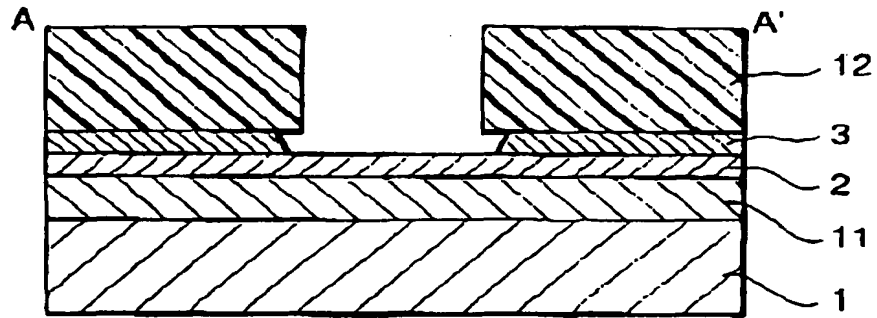


FIG. 10

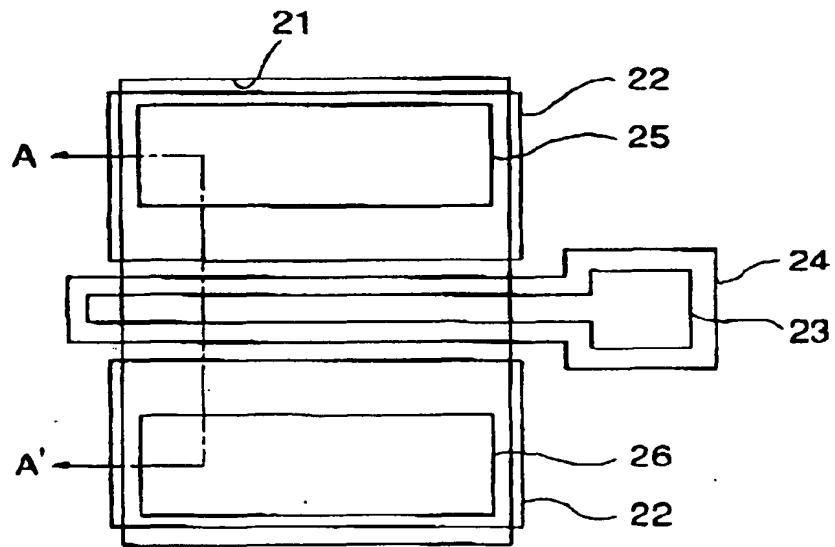


FIG. 11

FIG. 12A

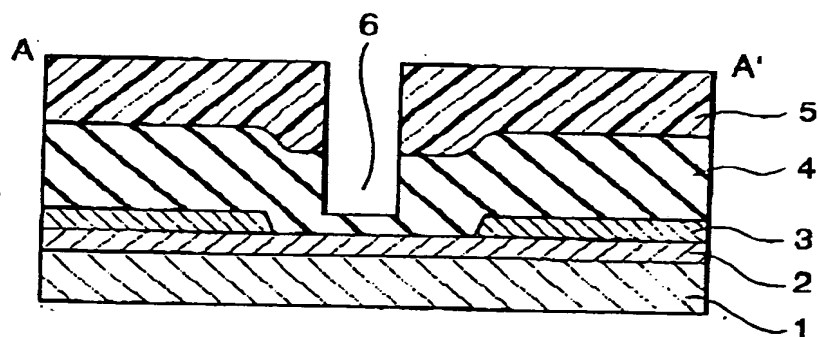


FIG. 12B

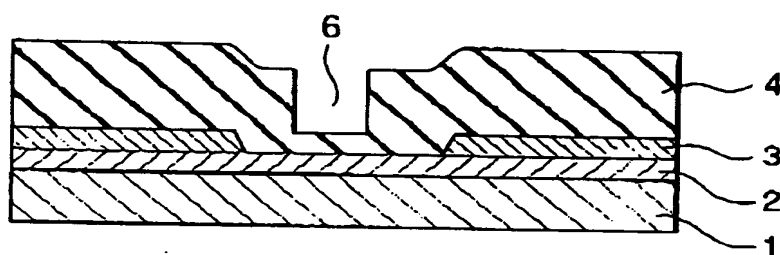


FIG. 12C

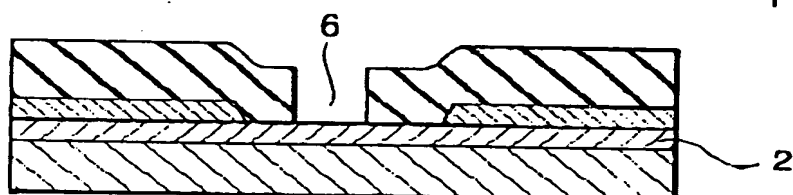


FIG. 12D

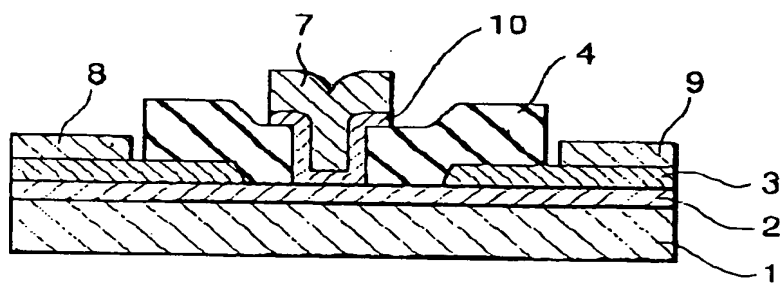


FIG. 13A

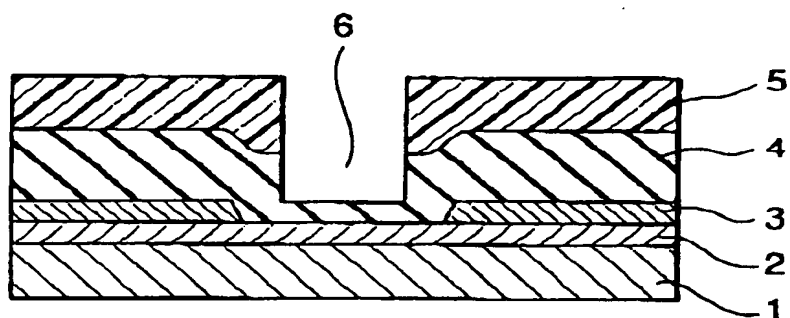


FIG. 13B

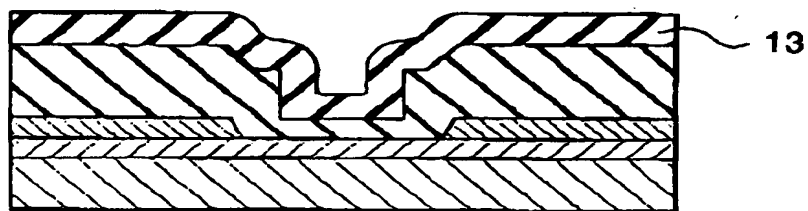


FIG. 13C

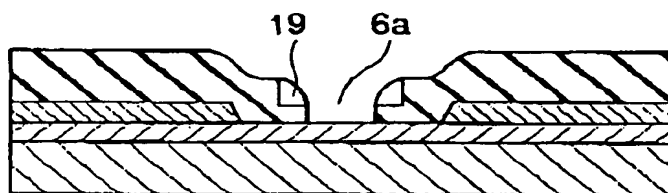
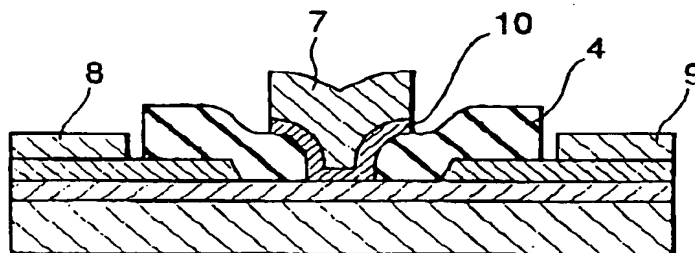


FIG. 13D



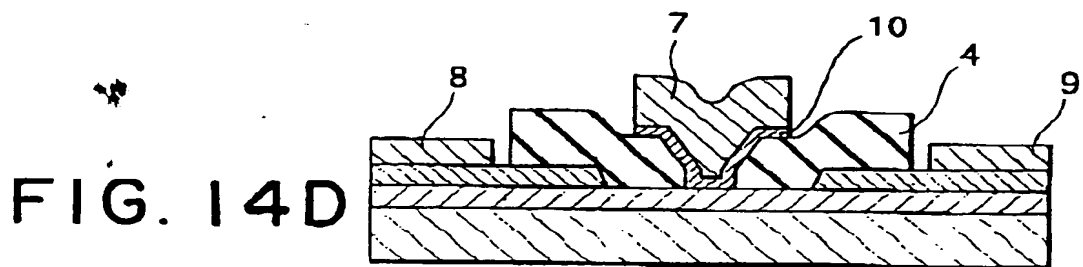
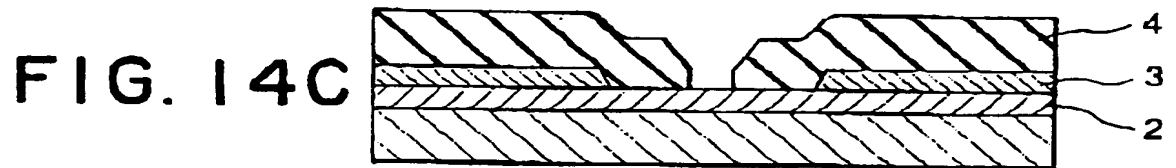
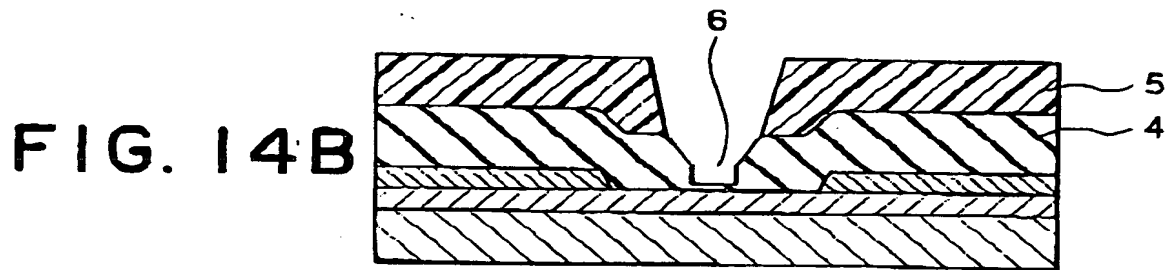
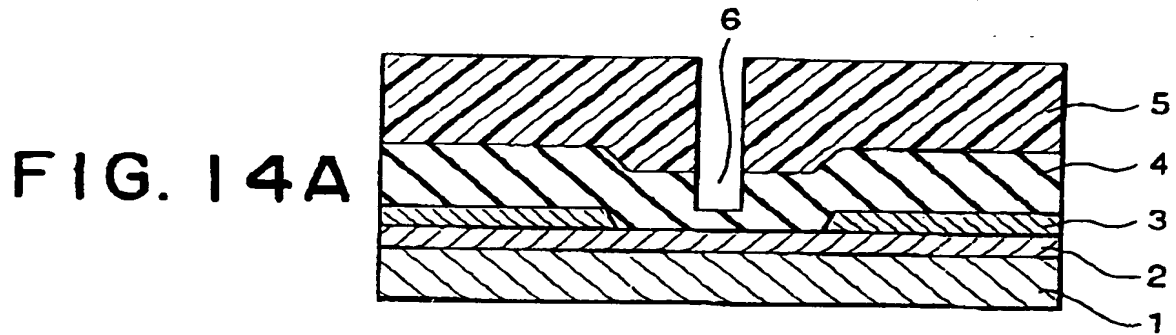


FIG. 15A

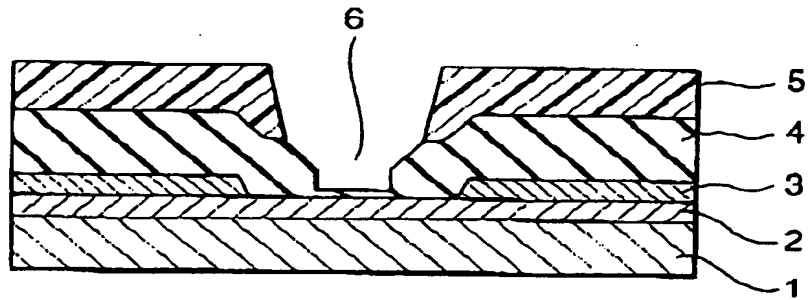


FIG. 15B

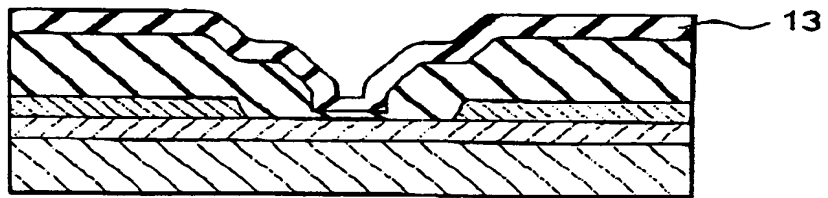


FIG. 15C

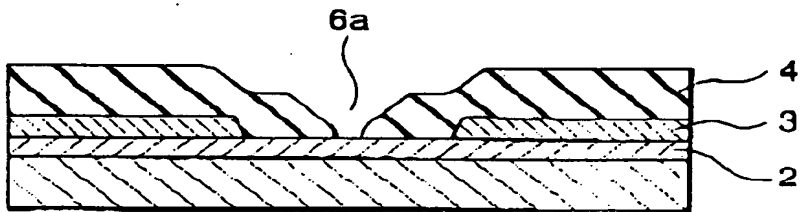


FIG. 15D

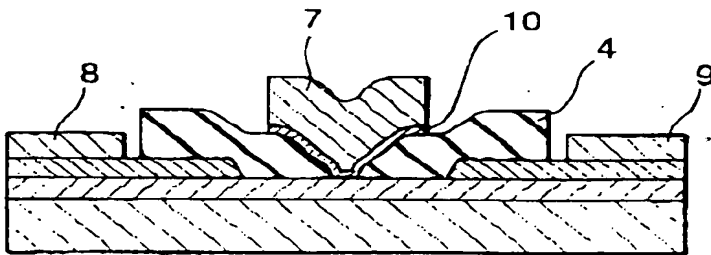


FIG. 16A

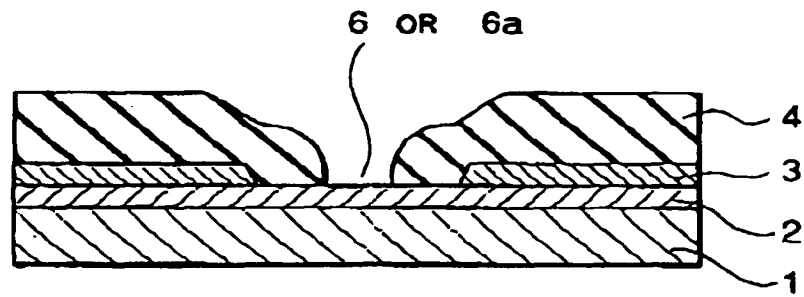


FIG. 16B

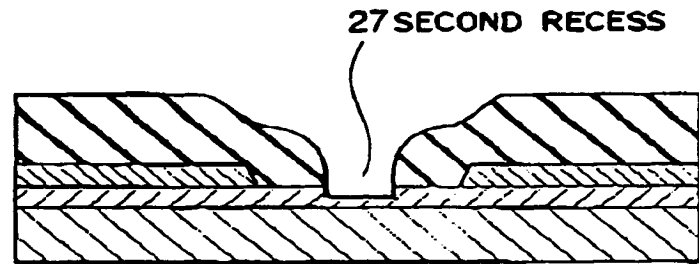


FIG. 16C

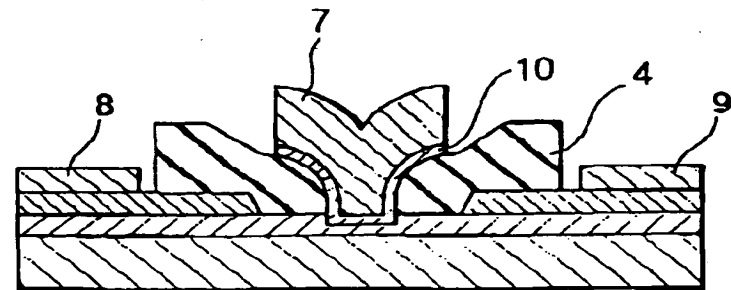


FIG. 17A

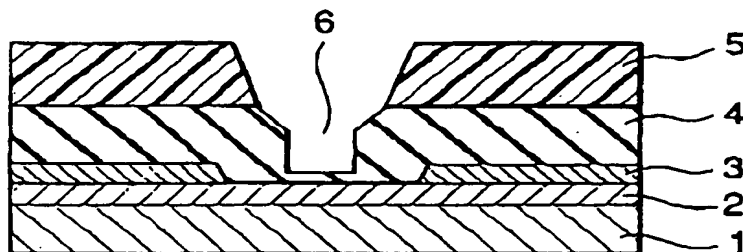


FIG. 17B

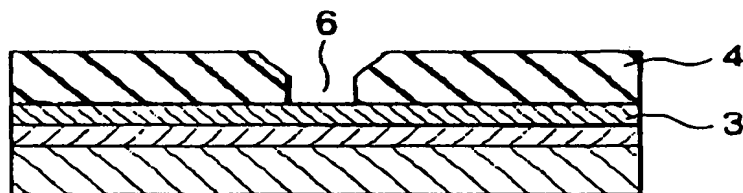


FIG. 17C

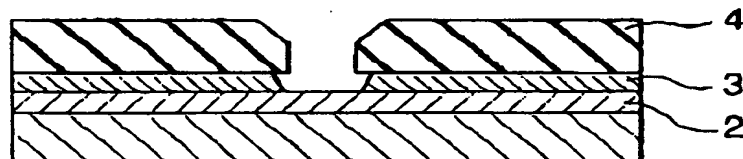


FIG. 17D

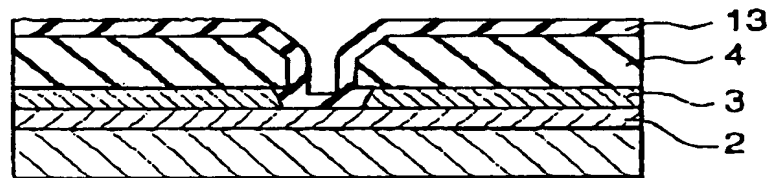


FIG. 17E

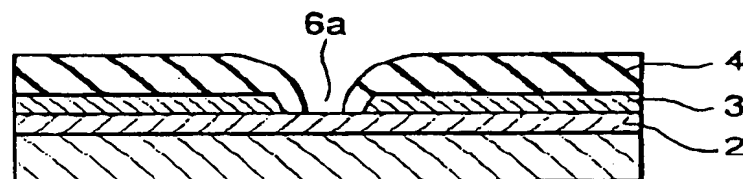


FIG. 17F

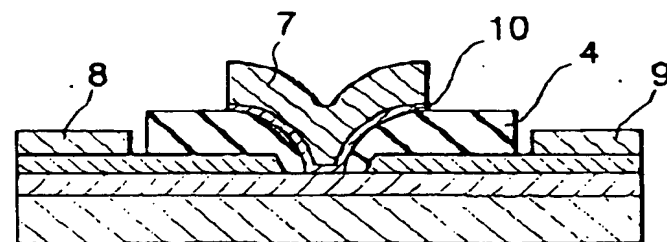


FIG. 18A

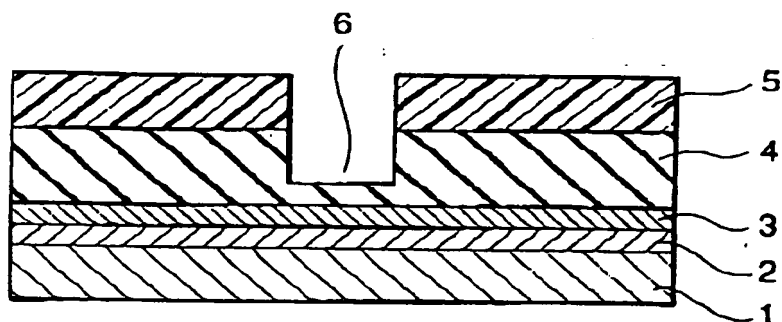


FIG. 18B

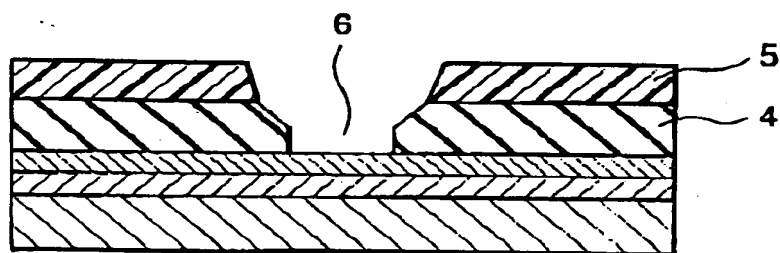


FIG. 18C

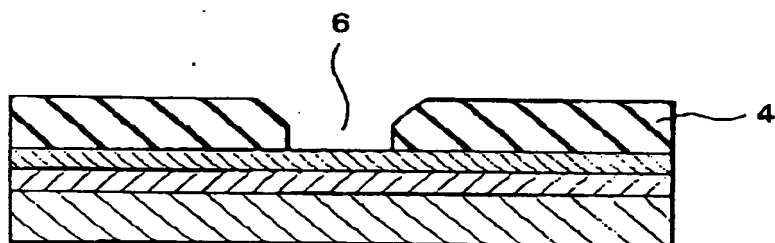


FIG. 18D

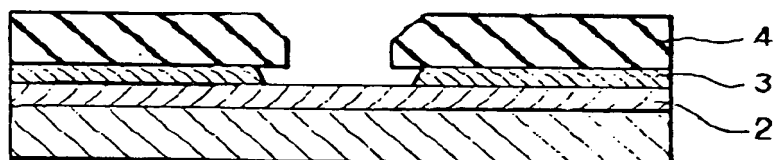


FIG. 19A

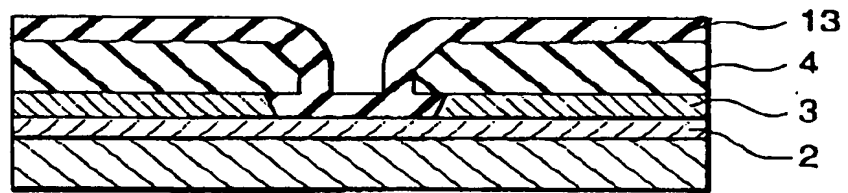


FIG. 19B

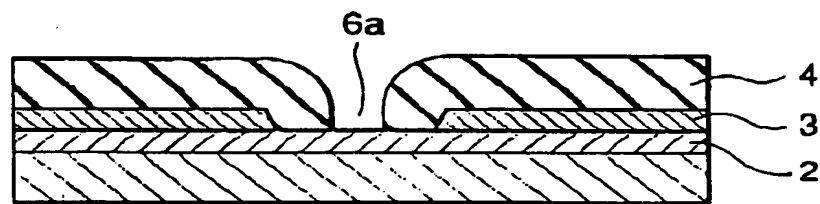


FIG. 19C

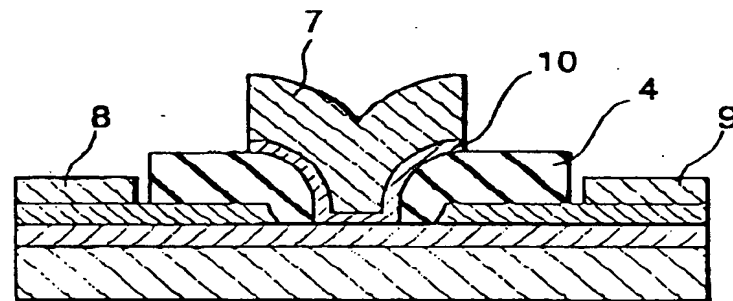


FIG. 20A

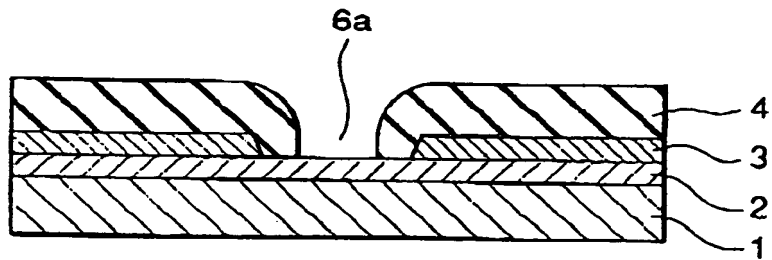


FIG. 20B

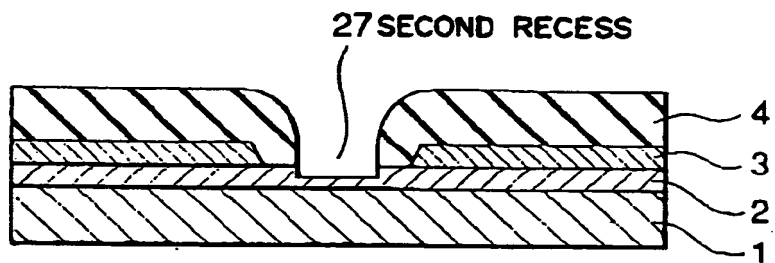
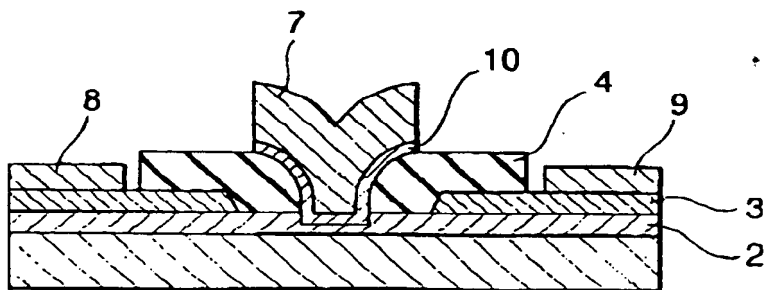


FIG. 20C



(19)



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(11)

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(30) Priority: **28.08.1997 JP 23195597**

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(54) Method of manufacturing a field effect transistor

(57) In a method of manufacturing a semiconductor device which has a semiconductor substrate, a channel layer formed on the semiconductor substrate and an insulating film deposited on the channel layer, an opening corresponding to a gate electrode pattern is formed in the insulating film by the use of a photo-resist film. The channel layer contains crystal components while

the photo-resist film contains carbon. The insulating film is etched to exposed said channel layer after removing the photo-resist film. In consequence, no reacted production is formed between the crystal components and the carbon on the exposed channel layer.

FIG. 12A

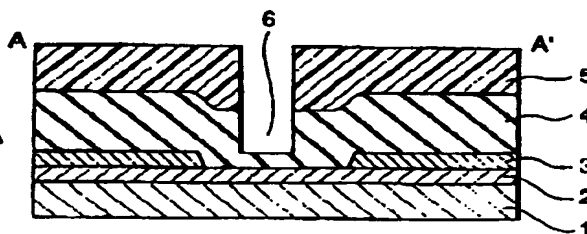
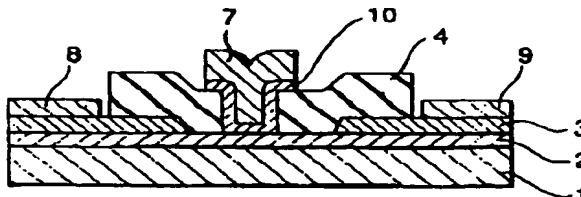


FIG. 12D



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PARTIAL EUROPEAN SEARCH REPORT

Application Number

which under Rule 45 of the European Patent Convention shall be considered, for the purposes of subsequent proceedings, as the European search report

EP 98 11 6263

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	HIDA H ET AL: "A 0.25 μ m inner sidewall-assisted super self-aligned gate heterojunction FET fabricated using all dry-etching technology for low voltage controlled LSIs" INTERNATIONAL ELECTRON DEVICES MEETING 1992. TECHNICAL DIGEST, SAN FRANCISCO, CA, USA, 13 - 16 December 1992, pages 982-984, XP000687590 IEEE, New York, USA ISBN: 0-7803-0817-4 * page 982; figure 1 *	1-3,5,6, 8-14,16, 20,21,24	H01L21/338 H01L21/335 H01L21/28 H01L29/10
A	METZE G M ET AL: "A dielectric-defined process for the formation of T-gate field-effect transistors" IEEE MICROWAVE AND GUIDED WAVE LETTERS, vol. 1, no. 8, August 1991 (1991-08), pages 198-200, XP000209511 ISSN: 1051-8207 section II. "Material growth and device fabrication"	1-3,5,6, 8,10,16, 20,24	<div>TECHNICAL FIELDS SEARCHED (Int.Cl.6)</div> <div>H01L</div>
INCOMPLETE SEARCH			
<p>The Search Division considers that the present application, or one or more of its claims, does/do not comply with the EPC to such an extent that a meaningful search into the state of the art cannot be carried out, or can only be carried out partially, for these claims.</p> <p>Claims searched completely :</p> <p>Claims searched incompletely :</p> <p>Claims not searched :</p> <p>Reason for the limitation of the search:</p> <p>see sheet C</p>			
Place of search		Date of completion of the search	Examiner
THE HAGUE		18 August 2000	Köpf, C
<div>CATEGORY OF CITED DOCUMENTS</div> <div> <p>X : particularly relevant if taken alone</p> <p>Y : particularly relevant if combined with another document of the same category</p> <p>A : technological background</p> <p>O : non-written disclosure</p> <p>P : intermediate document</p> </div> <div> <p>T : theory or principle underlying the invention</p> <p>E : earlier patent document, but published on, or after the filing date</p> <p>D : document cited in the application</p> <p>L : document cited for other reasons</p> <p>& : member of the same patent family, corresponding document</p> </div>			

EPO FORM 1503 03/82 (P/M/C07)



European Patent
Office

**INCOMPLETE SEARCH
SHEET C**

Application Number
EP 98 11 6263

Claim(s) searched completely:
1-23

Reason for the limitation of the search:

Claim 24 in its present form is unclear. Since it can only be understood in conjunction with a two-step etching process of the insulating film with intermediate photo-resist removal step as described in claim 1, search has been performed correspondingly.

Furthermore it has been assumed that the term "channel layer contains crystal components" means a crystalline semiconductor channel layer as is commonly known in the art, and "photo-resist film contains carbon" means a commonly used (organic) photo-resist.

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